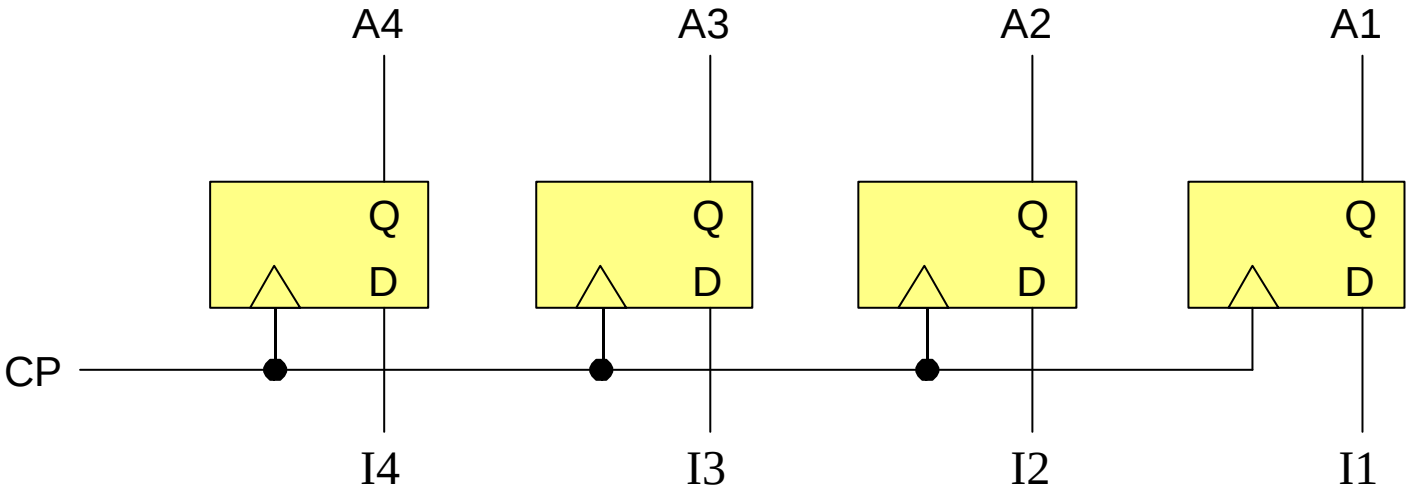
7장 Register, Counter and Memory

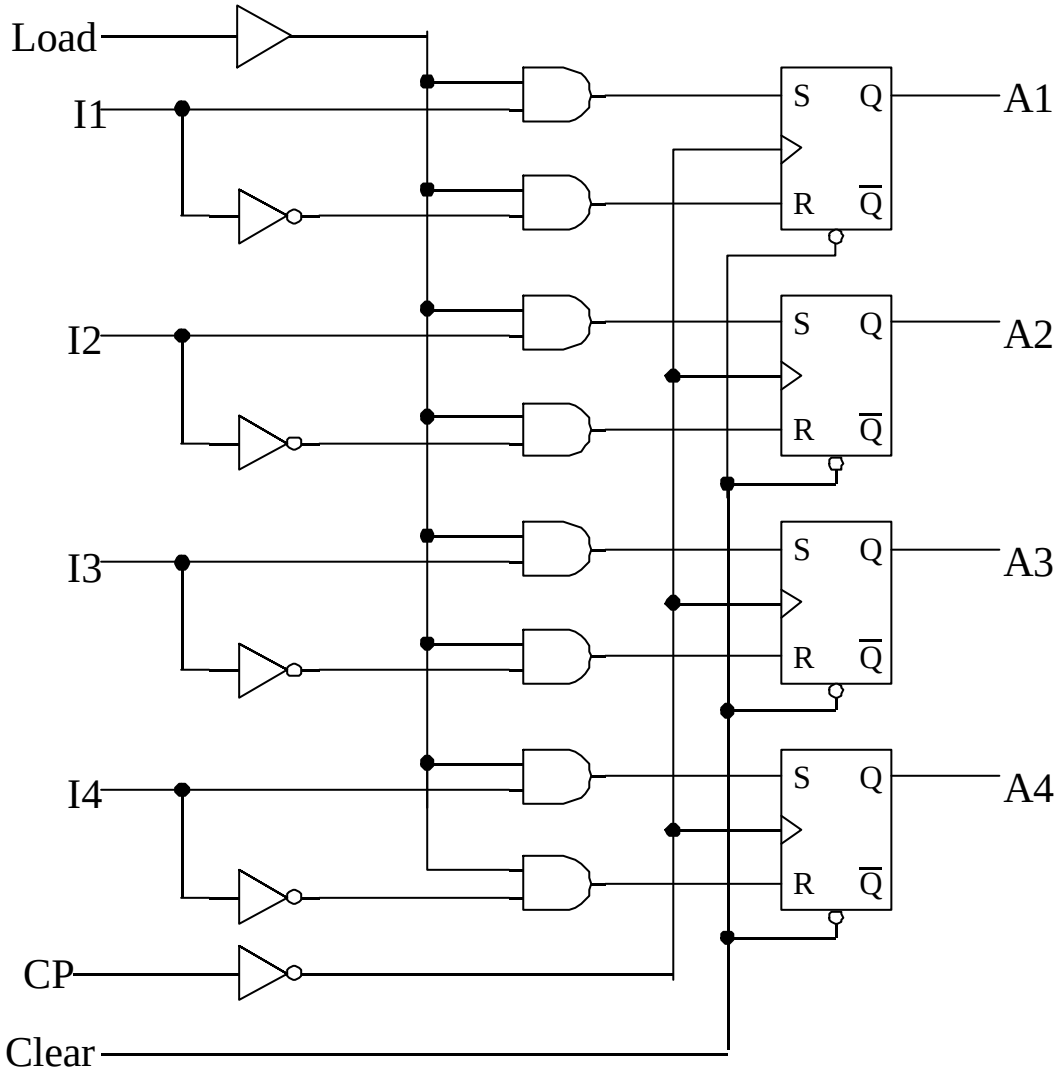
Register and Counter

- Register : 2진정보를 기억하기 위한 binary cell들의 집합
  FF과 combinational gate들로 구성
- Counter : Special case of register

- 4 bit register : parallel load

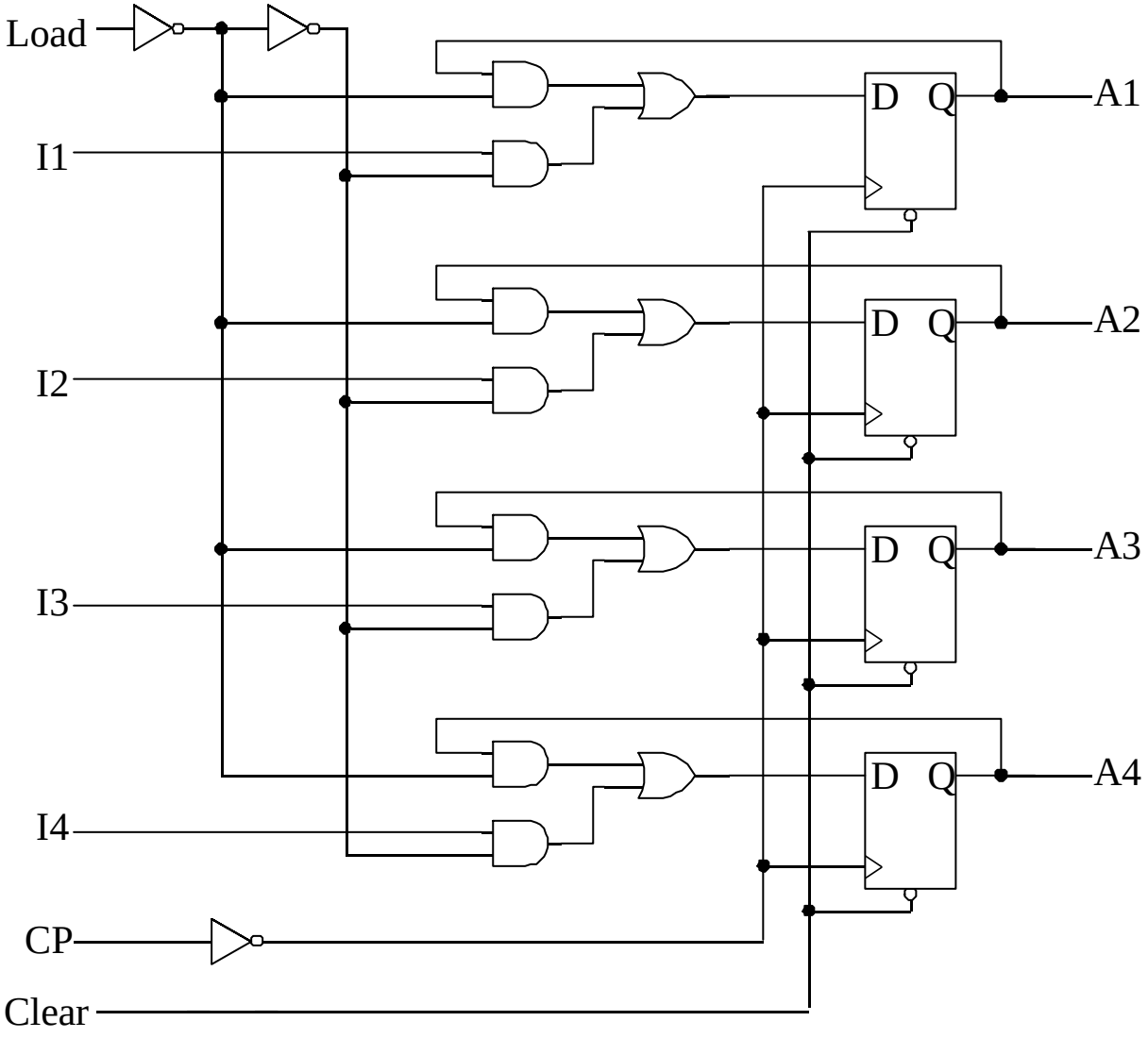


4 Bits Register with Parallel Load (RS FF)



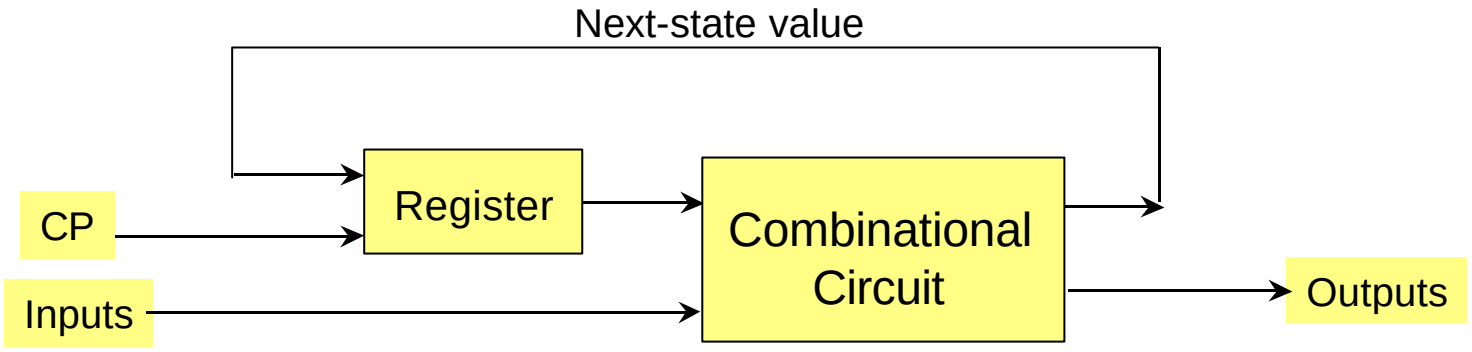
Clear	CP	Load	Function
0	X	X	clear to 0
1	X	0	no change
1	↓	1	load input

4 Bits Register with Parallel Load (D FF)



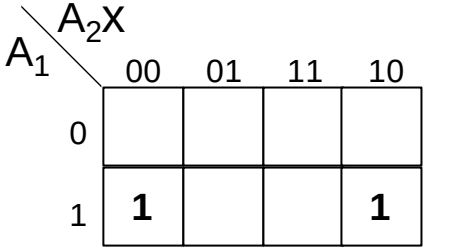
Clear	CP	Load	Function
0	X	X	clear to 0
1	X	0	no change
1	↓	1	load input

Sequential Logic Design with Register

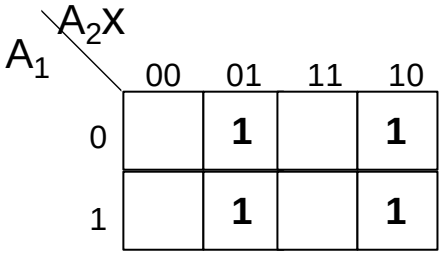


Sequential Logic Design with Register

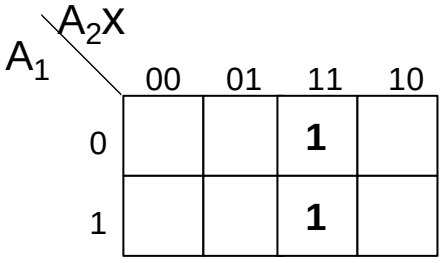
현재상태	입력	다음상태	출력
A1 A2	x	A1 A2	y
0 0	0	0 0	0
0 0	1	0 1	0
0 1	0	0 1	0
0 1	1	0 0	1
1 0	0	1 0	0
1 0	1	0 1	0
1 1	0	1 1	0
1 1	1	0 0	1



$A_1 = A_1 x'$



$A_2 = A_2' x + A_2 x = A_2 \oplus x$



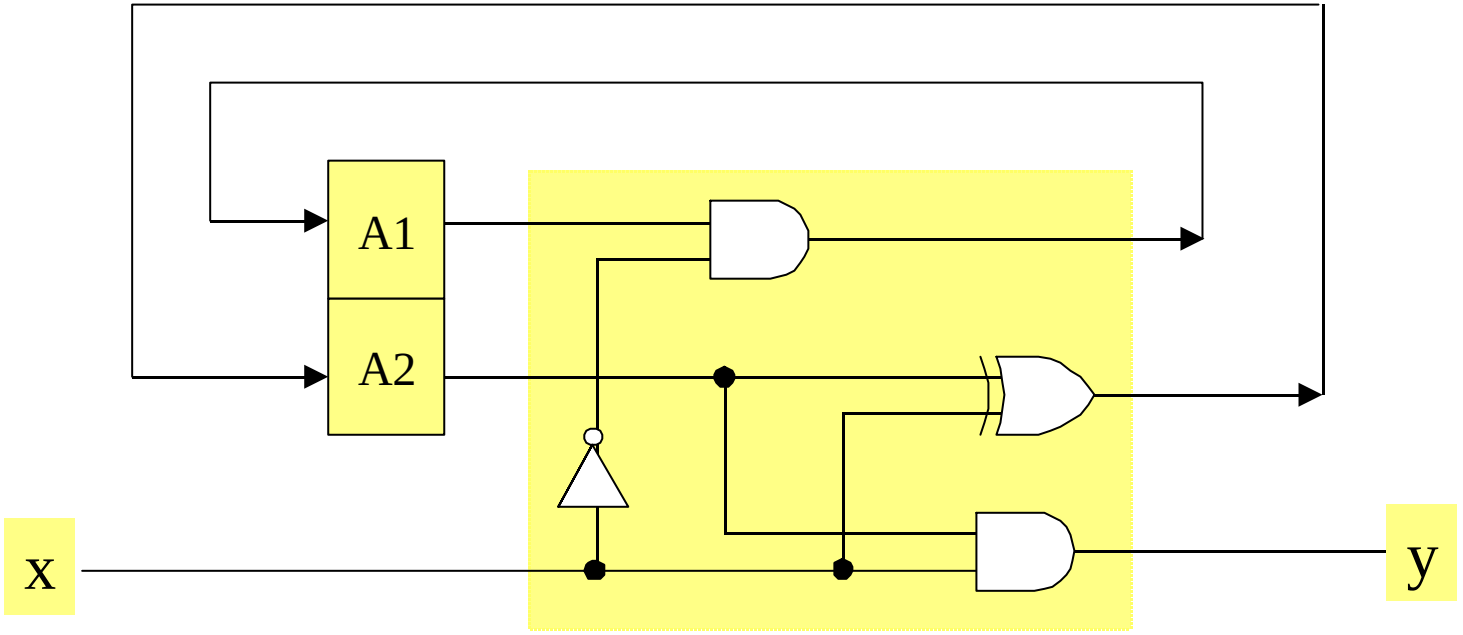
$y = A_2 x$

Sequential Logic Design with Register

$A_1 = A_1 x'$

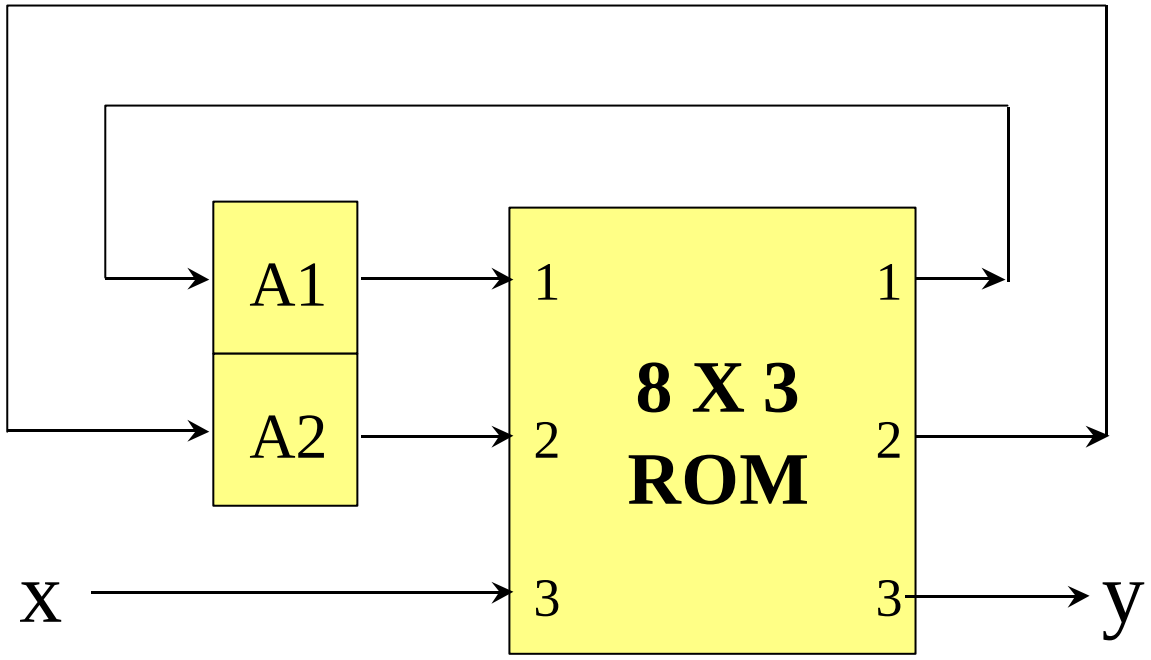
$A_2 = A_2' x + A_2 x = A_2 \oplus x$

$y = A_2 x$



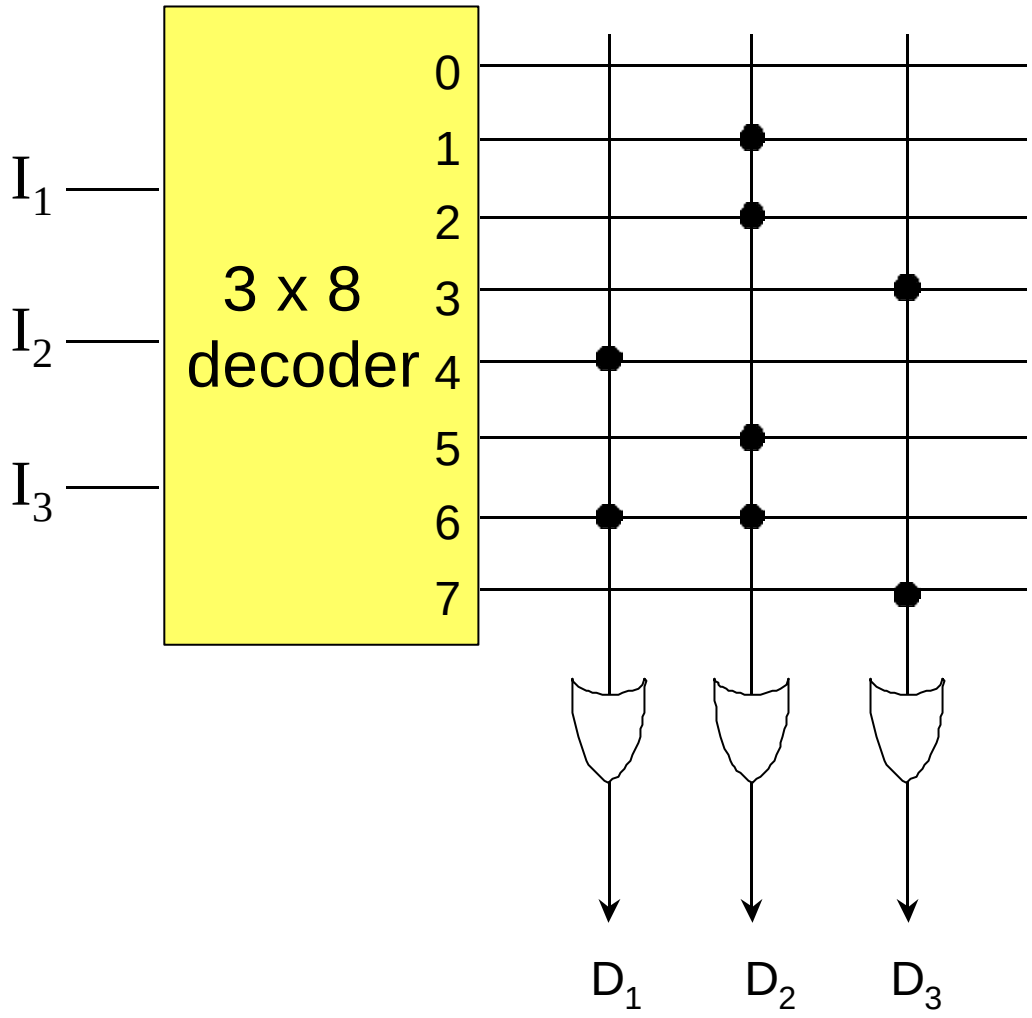
Sequential Logic Design with Register+ROM

Address			Output		
1	2	3	1	2	3
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	0	1
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1



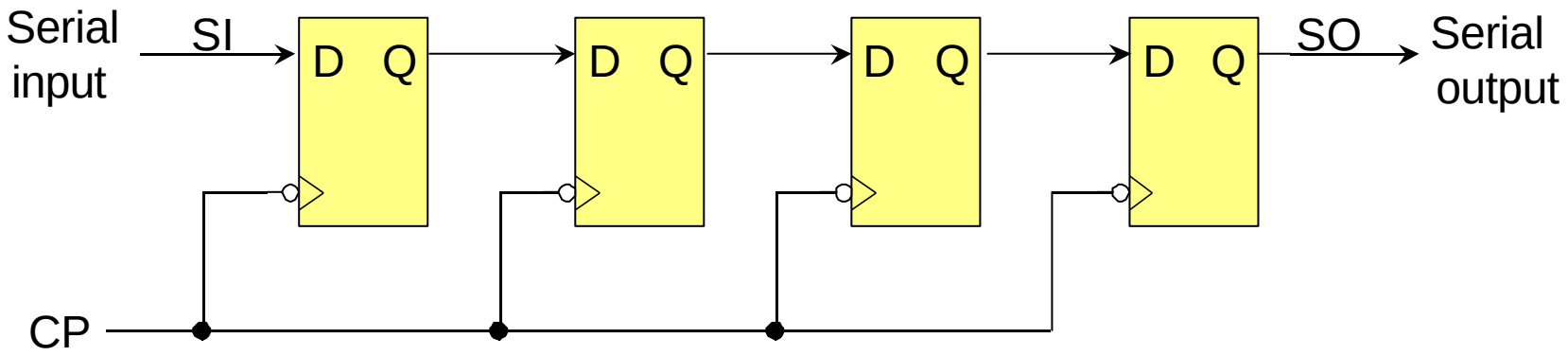
8x3 ROM Programming

Address			Output		
1	2	3	1	2	3
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	0	1
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

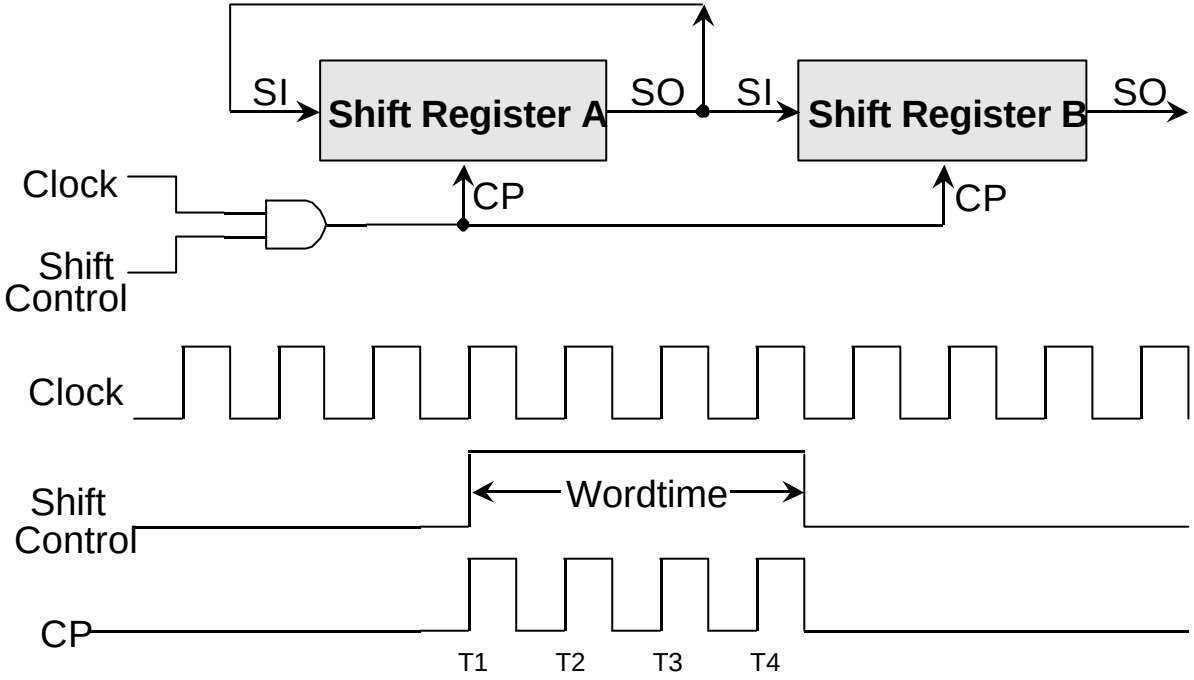


Shift Register

- Shift register : 2진정보를 좌우측으로 이동(shift)시키는 레지스터
- Register의 형태
  - PIPO (Parallel Input Parallel Output)
  - PISO (Parallel Input Serial Output)
  - SIPO (Serial Input Parallel Output)
  - SISO (Serial Input Serial Output)



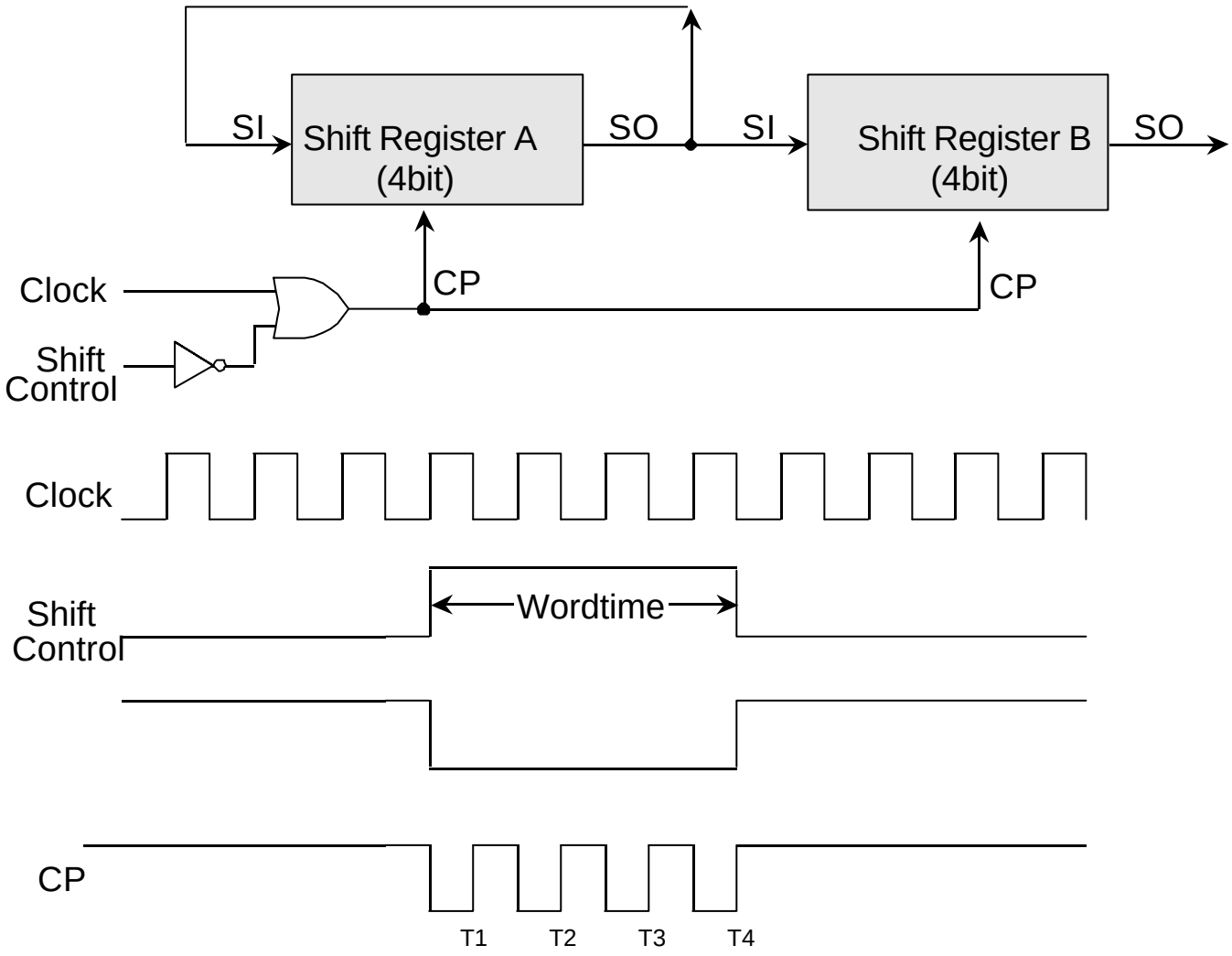
Serial Transfer



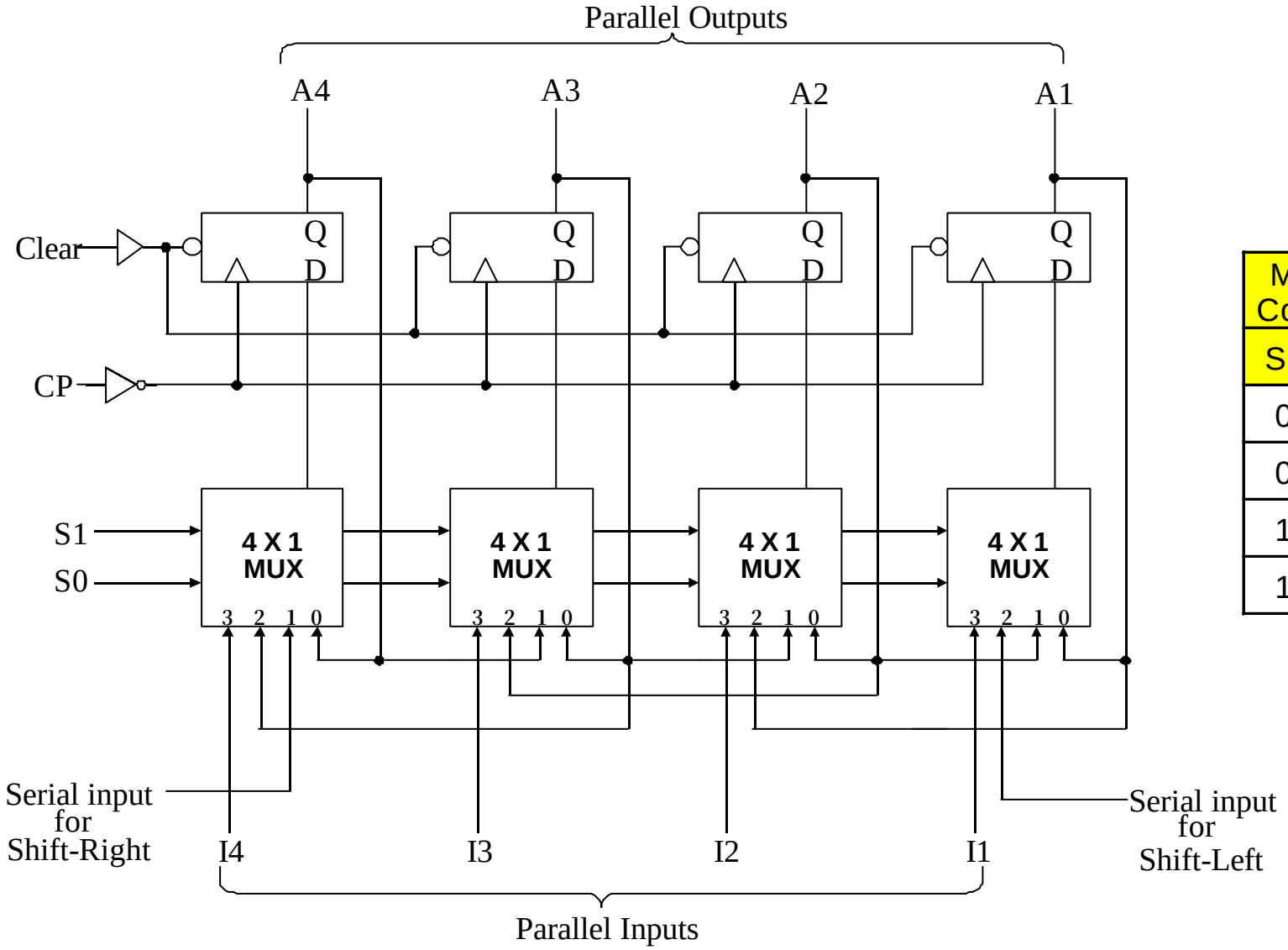
- Source register에서 destination register로 한번에 1 bit씩 이동
- Source register의 정보손실을 막기 위하여 source register의 내용을 순환

Timing Pulse	Shift Register A	Shift Register B	Serial Output of B
Initial Value	1 0 1 1	0 0 1 0	0
After T1	1 1 0 1	1 0 0 1	1
After T2	1 1 1 0	1 1 0 0	0
After T3	0 1 1 1	0 1 1 0	0
After T4	1 0 1 1	1 0 1 1	1

Serial Transfer

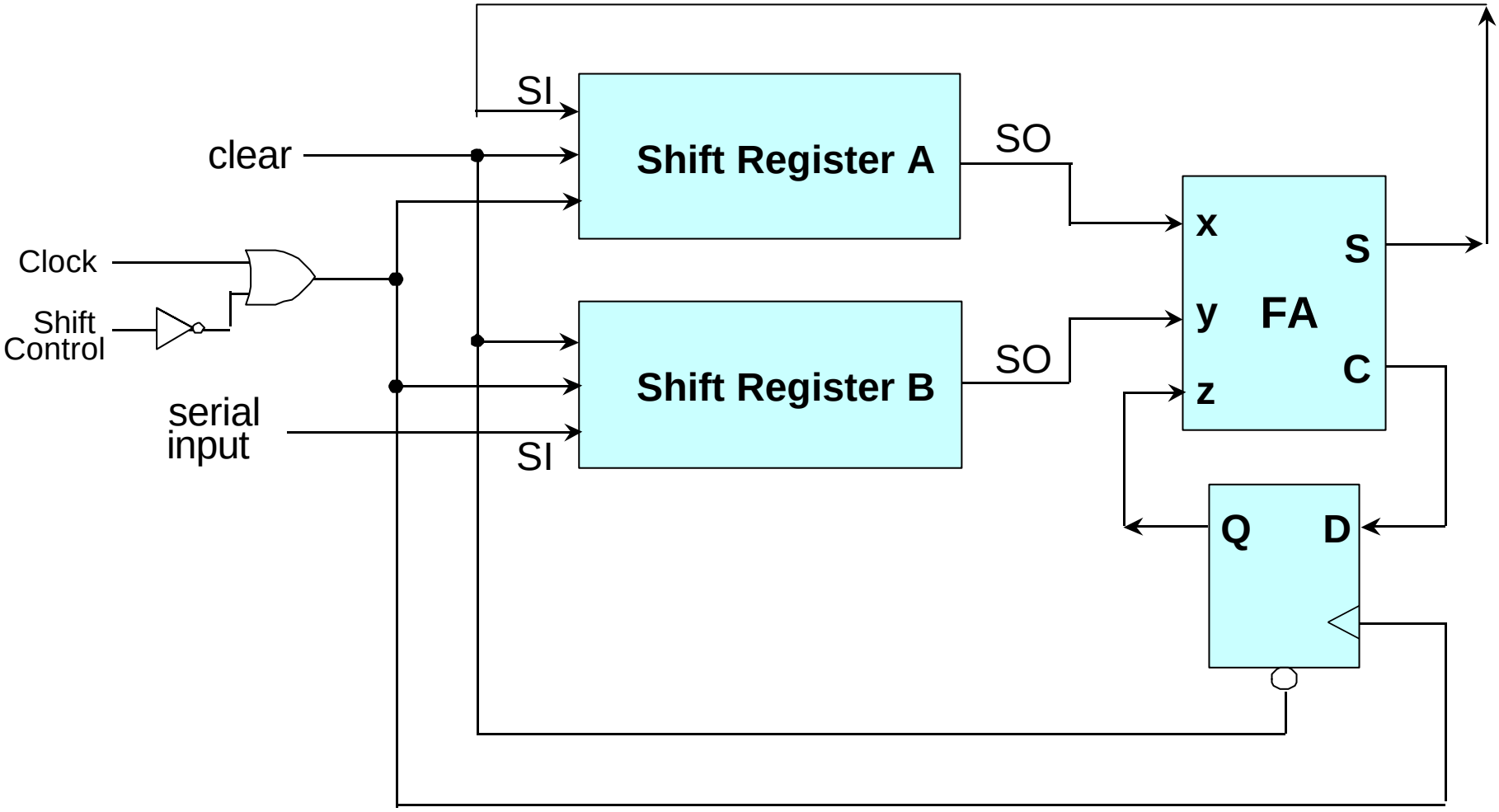


Bidirectional Shift Register with Parallel Load

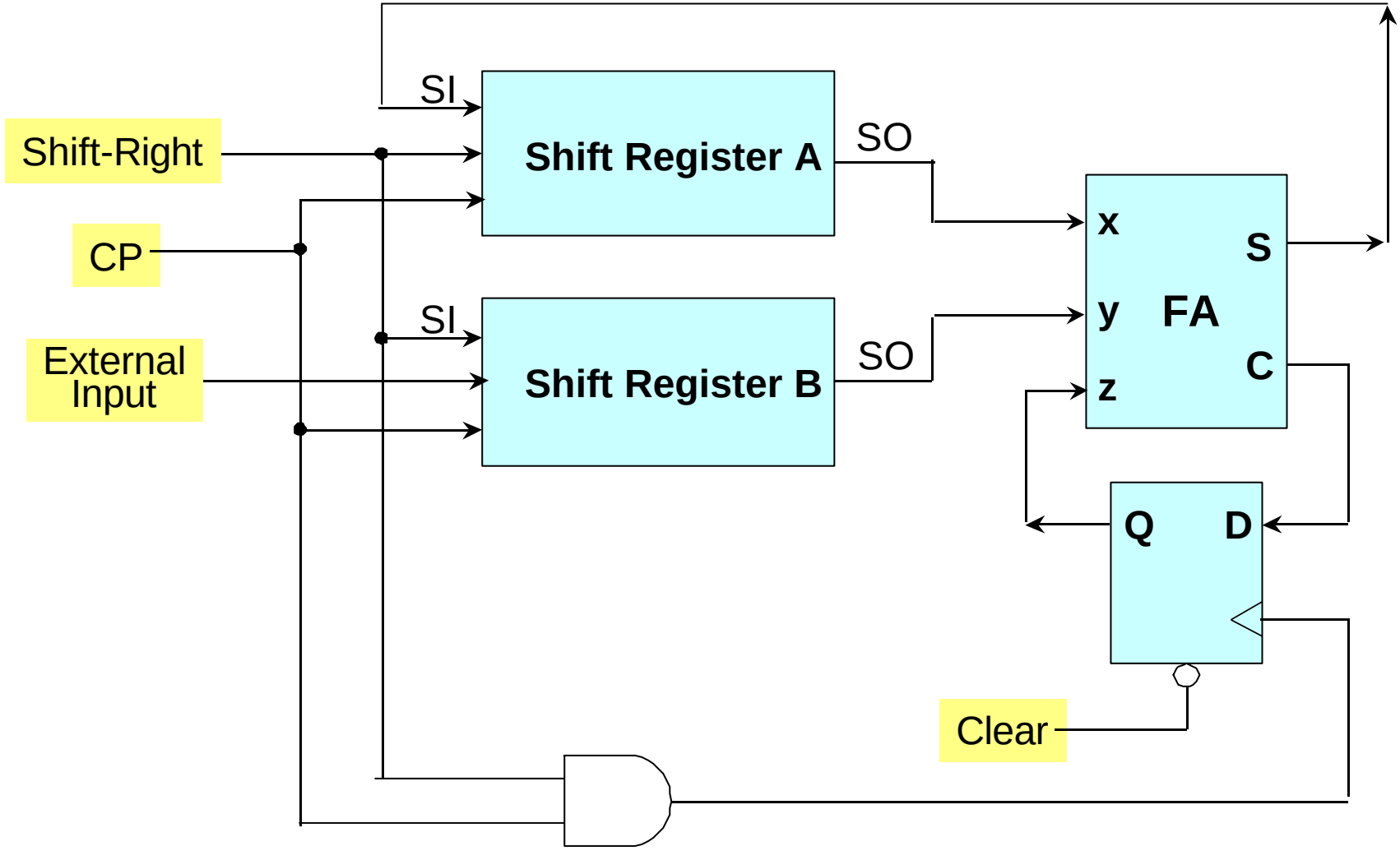


Mode Control		Register operation
S1	S0	
0	0	no change
0	1	shift right
1	0	shift left
1	1	parallel load

Serial Adder with Full Adder

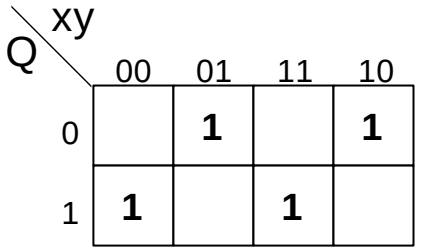


Serial Adder with Full Adder

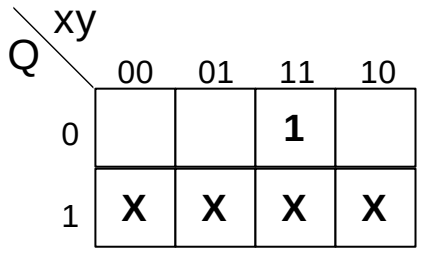


Serial Adder Design with JK FF

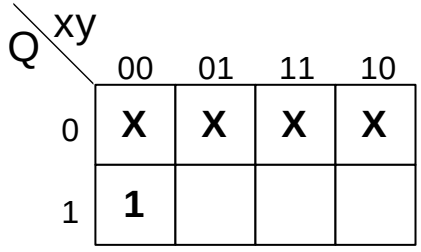
현재 상태	입력		다음 상태	출력	Flip Flop 입력	
Q	x	y	Q	S	JQ	KQ
0	0	0	0	0	0	X
0	0	1	0	1	0	X
0	1	0	0	1	0	X
0	1	1	1	0	1	X
1	0	0	0	1	X	1
1	0	1	1	0	X	0
1	1	0	1	0	X	0
1	1	1	1	1	X	0



$S = Q \oplus x \oplus y$



$JQ = xy$



$KQ = x' y' = \overline{x+y}$

Serial Adder Design with JK FF