Counter

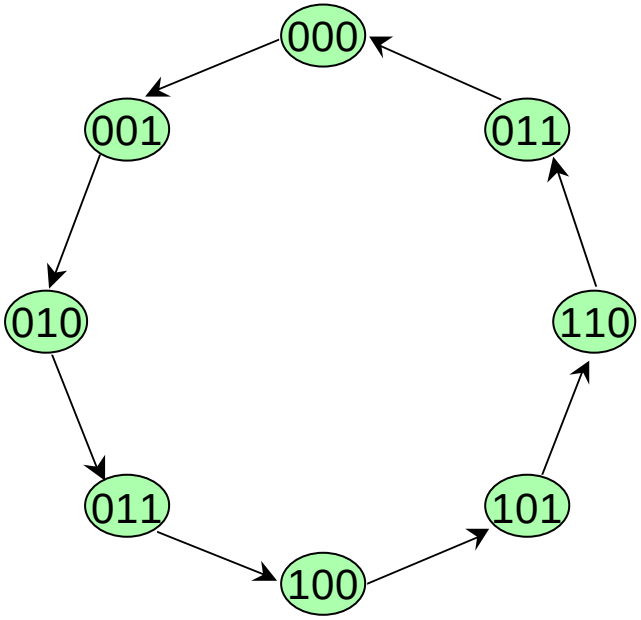
- 미리 정해진 순서대로 계수하는 회로
- FF들이 미리 정해진 순서를 따라 상태가 천이되도록 논리 설계

카운터의 분류

- FF의 상태변화 시기에 따라
  - 동기식카운터 : 모든 FF이 동일한 클럭펄스에 의해서 동시에 상태천이
  - 비동기식 카운터 : 다른 FF들의 출력 신호를 클럭으로 사용
- 세는 수의 범위에 따라
  - modulo-N, divide-by-N 카운터
  - arbitrary sequence
- 수를 세는 순서에 따라
  - up counter : 증가하는 순으로 계수
  - down counter : 감소하는 순으로 계수
  - up/down counter : 제어입력에 따라 증가, 또는 감소순으로 계수

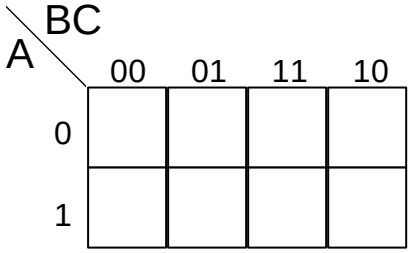
Counter Design

- 3 bit binary counter

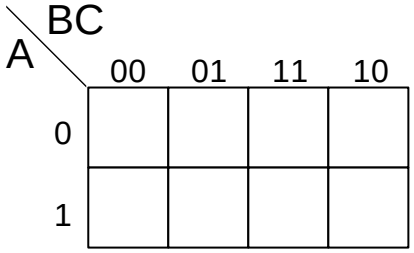


현재 상태	다음 상태	FF 입력		
A B C	A B C	T_A	T_B	T_C
0 0 0	0 0 1	0	0	1
0 0 1	0 1 0	0	1	1
0 1 0	0 1 1	0	0	1
0 1 1	1 0 0	1	1	1
1 0 0	1 0 1	0	0	1
1 0 1	1 1 0	0	1	1
1 1 0	1 1 1	0	0	1
1 1 1	0 0 0	1	1	1

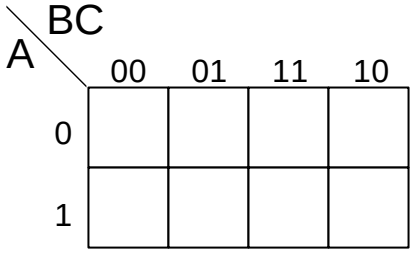
Counter Design



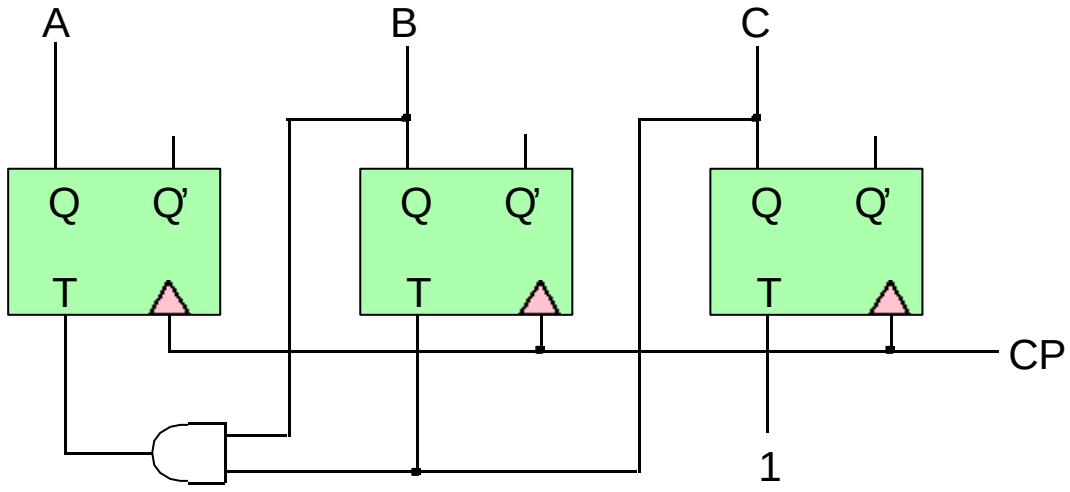
T_A=



T_B=

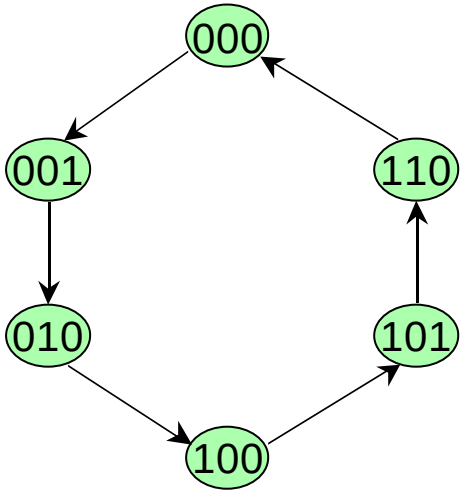


T_C=



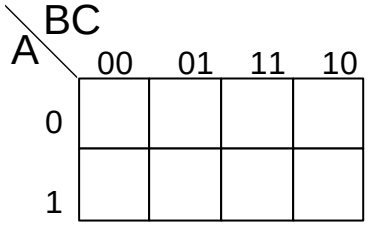
Counter Design

❑ 임의의 순서로 세는 카운터

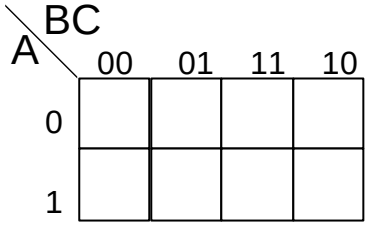


현재 상태	다음 상태	FF 입력		
A B C	A B C	J_A K_A	J_B K_B	J_C K_C
0 0 0	0 0 1			
0 0 1	0 1 0			
0 1 0	1 0 0			
1 0 0	1 0 1			
1 0 1	1 1 0			
1 1 0	0 0 0			

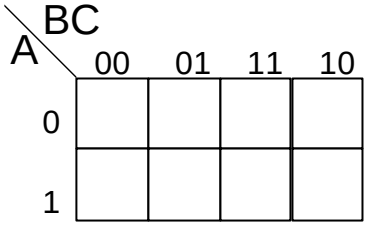
Counter Design



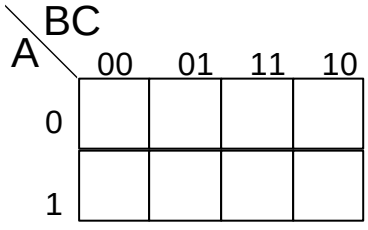
J_A=



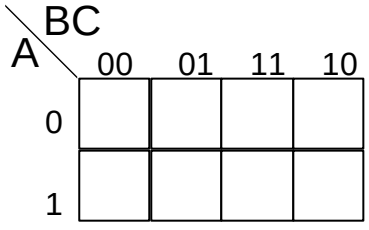
J_B=



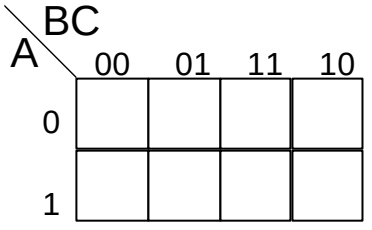
J_C=



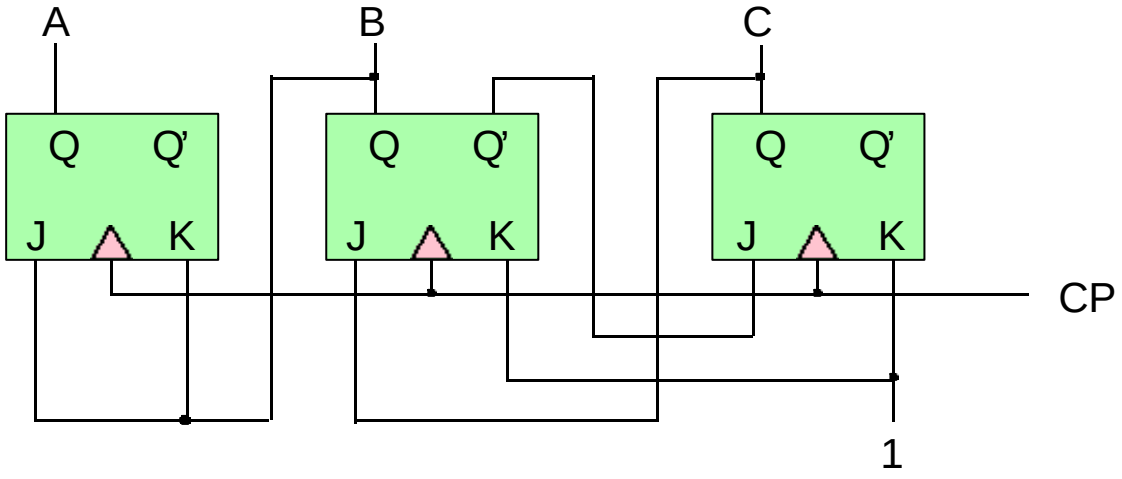
K_A=



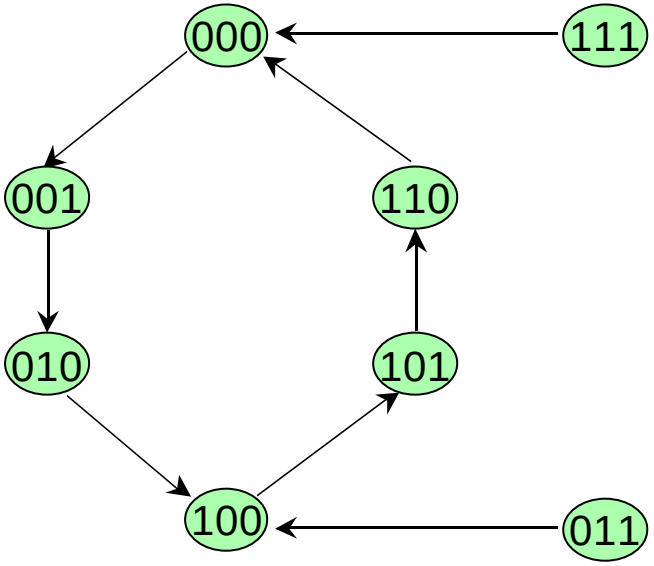
K_B=



K_C=



Counter Design

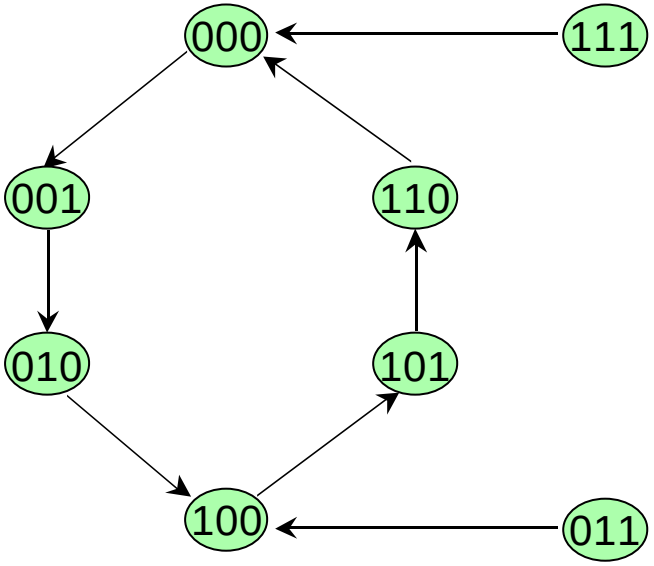


현재 상태	다음 상태	FF 입력		
A B C	A B C	J_A K_A	J_B K_B	J_C K_C
0 0 0				
0 0 1				
0 1 0				
0 1 1				
1 0 0				
1 0 1				
0 1 1				
1 1 1				

Counter Design

- 회로도

Counter Design



현재상태	다음상태	FF 입력		
A B C	A B C	T_A	T_B	T_C
0 0 0				
0 0 1				
0 1 0				
0 1 1				
1 0 0				
1 0 1				
0 1 1				
1 1 1				

Counter Design

- 회로도