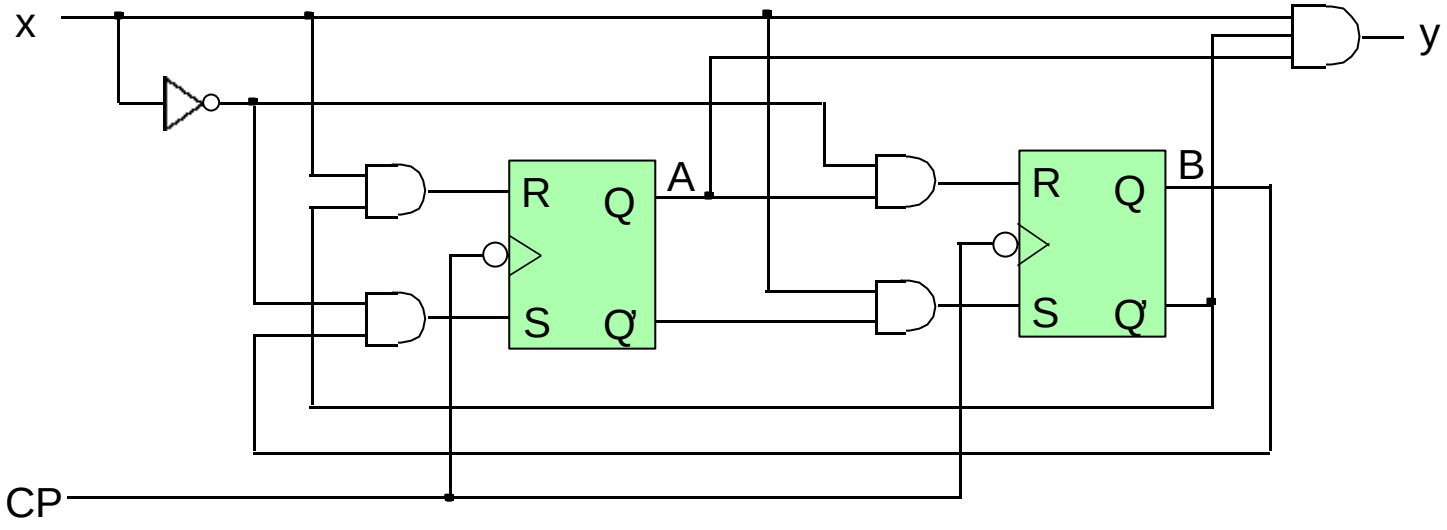
Sequential Circuit Analysis

(ex) **순차회로의 해석 예**



- **출력방정식**(output equation): **출력변수에 대한 표현식**

  $y = xAB'$

- Flip-flop **입력방정식**(FF input equation): flip-flop **입력단자에 대한 표현식**

  $R_A = xB'$, $S_A = x'B$

  $R_B = x'A$, $S_B = xA'$

Sequential Circuit Analysis

- **상태방정식**(state equation) : FF**의** state transition**을 표현한 대수식**

  RS flip-flop**의 특성방정식** $Q(t+1) = S+R'Q$

  $A(t+1) = S_A+R_A'A(t) = x'B + (xB')'A = x'B + (x'+B)A = x'B+x'A+AB$

  $B(t+1) = S_B+R_B'B(t) = xA' + (x'A)'B = xA' + (x+A')B = xA'+xB+A'B$

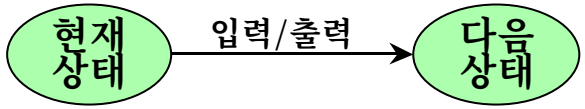
- **상태표**(state table): **현재상태, 입력, 다음상태, 출력을 표현한 표**

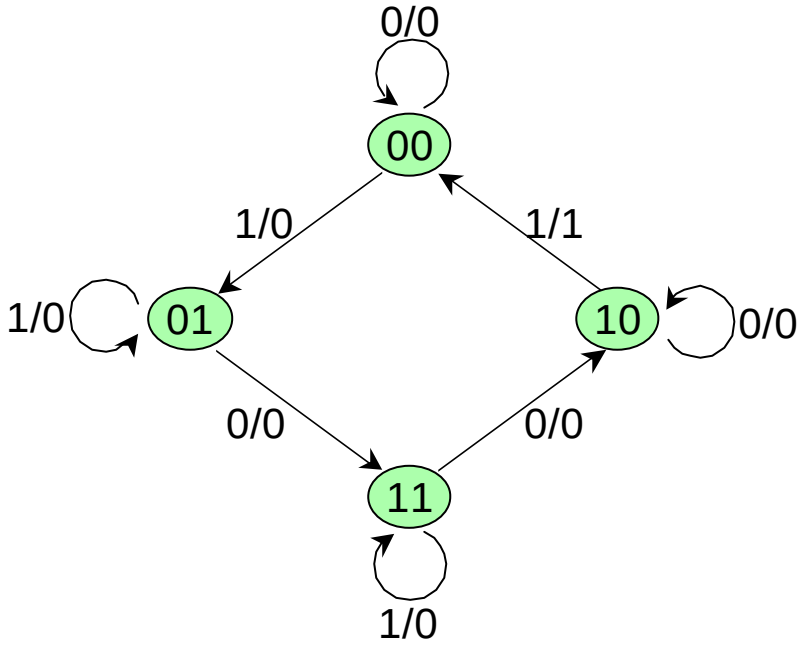
현재상태		입력	다음상태		출력
A	B	x	A	B	Y
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

현재	다음상태		출력	
상태	x=0	x=1	x=0	x=1
A B	A B	A B	y	y
0 0				
0 1				
1 0				
1 1				

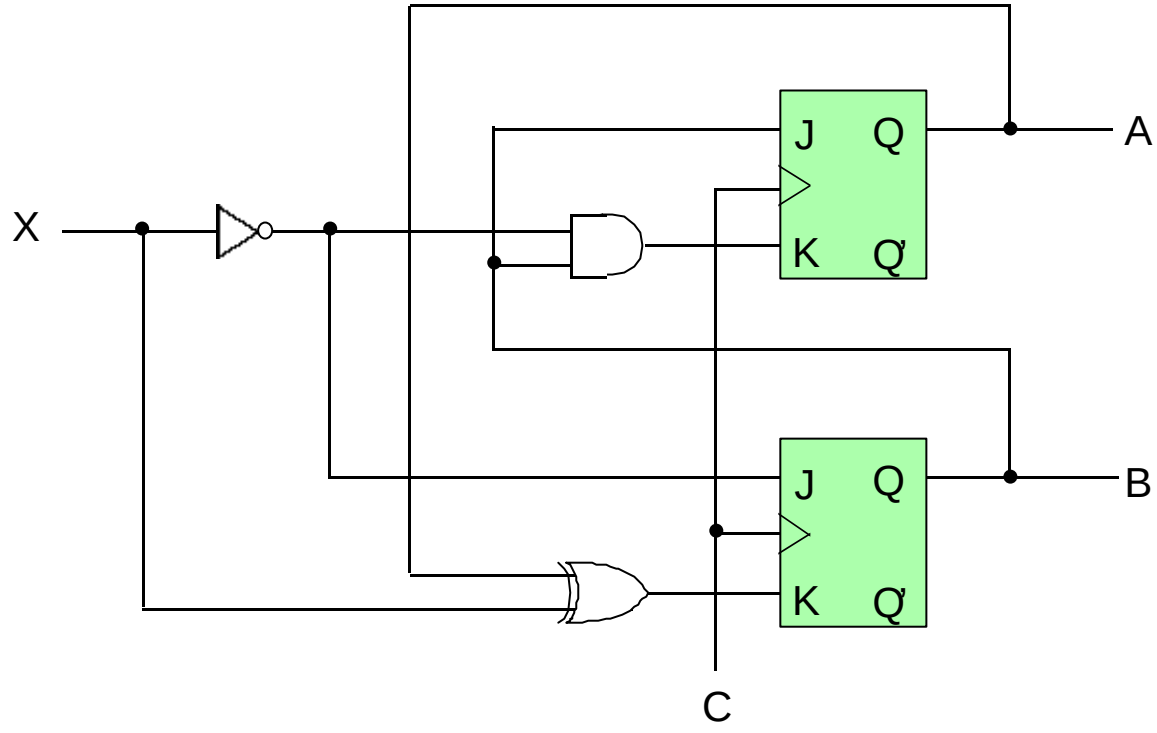
Sequential Circuit Analysis

◆ **상태도**(state diagram)





Sequential Circuit Analysis



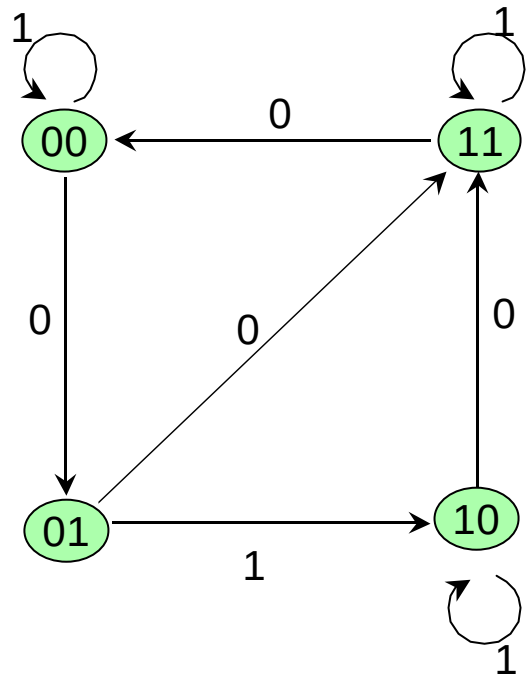
- FF input equation : $J_A = B$, $K_A = X'B$, $J_B = X'$, $K_B = X \oplus A$
- State equation
  - JK FF : $Q(t+1) = JQ' + K'Q$
  - $A(t+1) = BA' + (X'B)'A = BA' + XA + B'A = A \oplus B + XA$
  - $B(t+1) = X'B' + (X \oplus A)'B = X'B' + (X \oplus A)'B = X'B' + (X \odot A)B$

Sequential Circuit Analysis

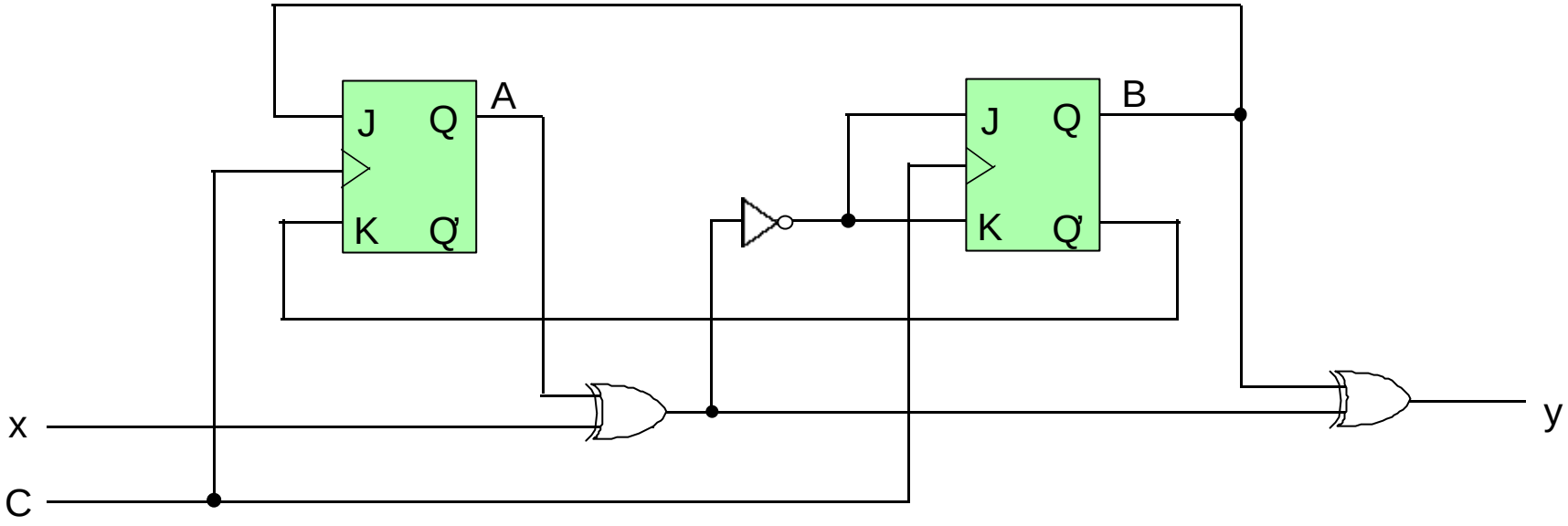
- State table

현재상태		입력	다음상태	
A	B	x	A	B
0	0	0	0	1
0	0	1	0	0
0	1	0	1	1
0	1	1	1	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	1	1

- State diagram



Sequential Circuit Analysis



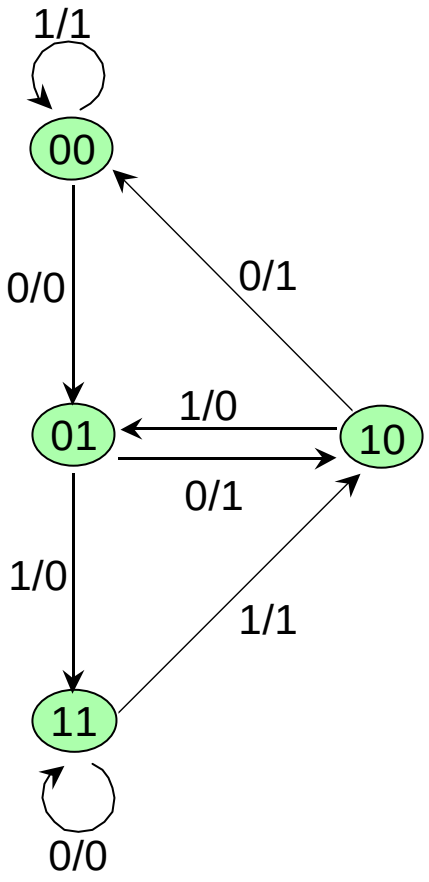
- output equation : $y = X \oplus A \oplus B$
- FF input equation : $J_A = B$, $K_A = B'$, $J_B = X \odot A$, $K_B = X \odot A$
- State equation
  - JK FF : $Q(t+1) = JQ' + K'Q$
  - $A(t+1) = BA' + BA = B$
  - $B(t+1) = (X \odot A)B' + (X \odot A)'B = (X \odot A) \oplus B = (X \oplus A)' \oplus B = (X \oplus A \oplus B)'$

Sequential Circuit Analysis

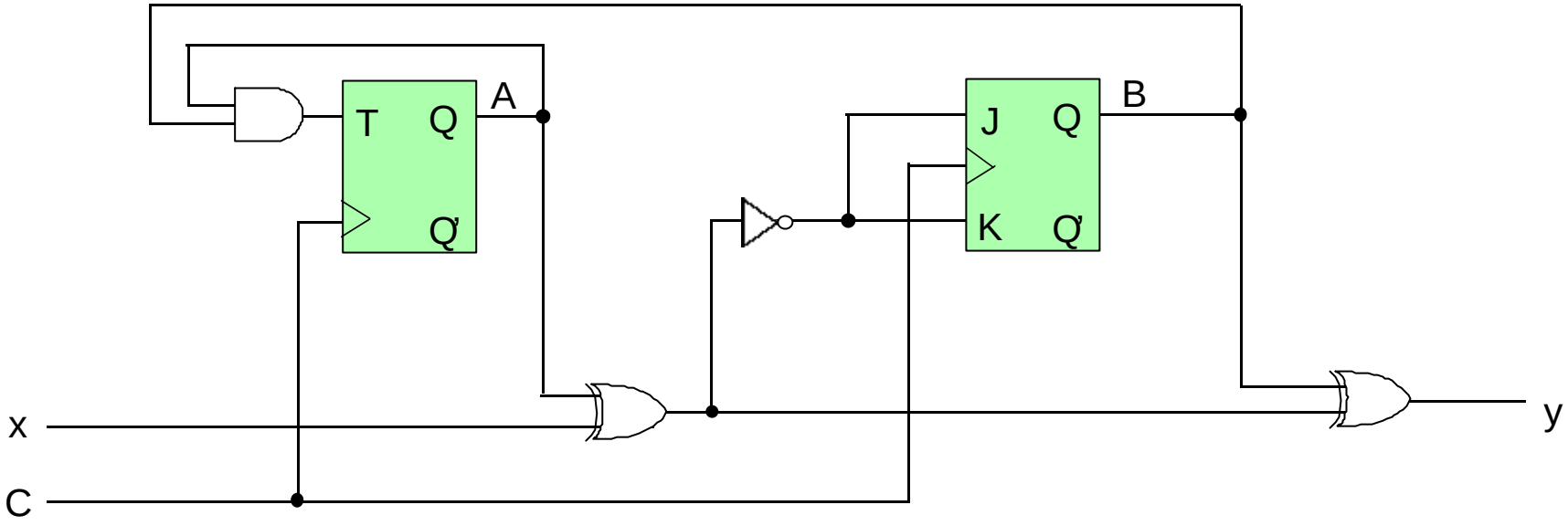
- State table

현재상태		입력	다음상태		출력
A	B	x	A	B	Y
0	0	0	0	1	0
0	0	1	0	0	1
0	1	0	1	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	1	0	1

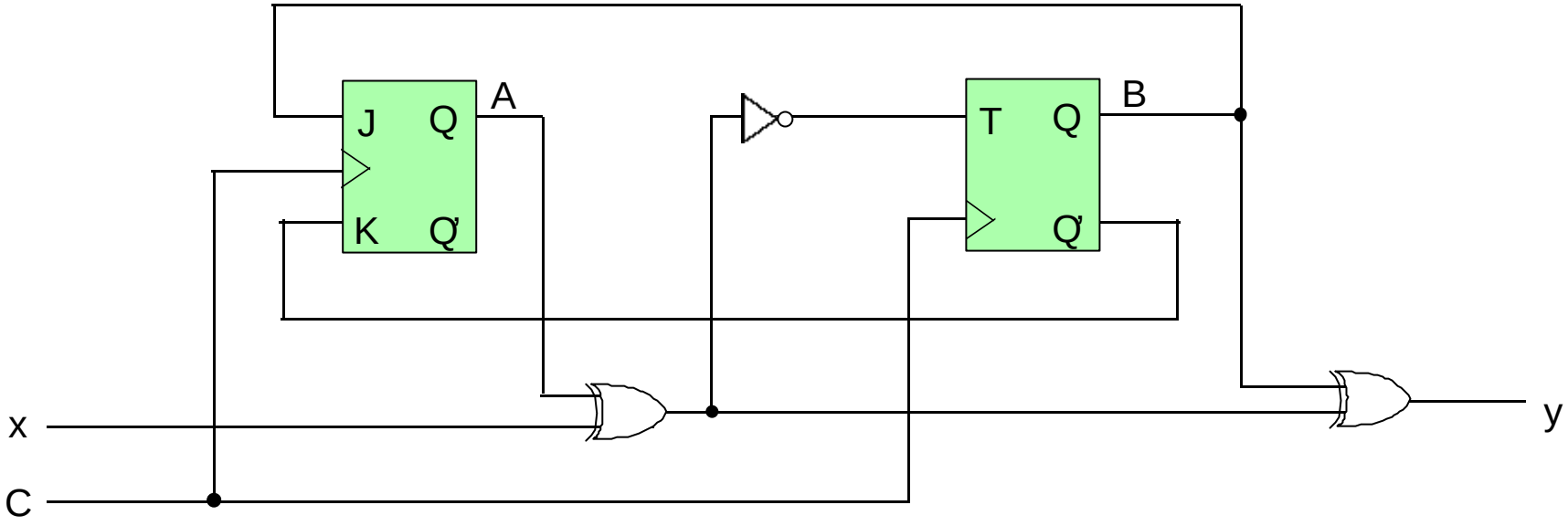
- State diagram



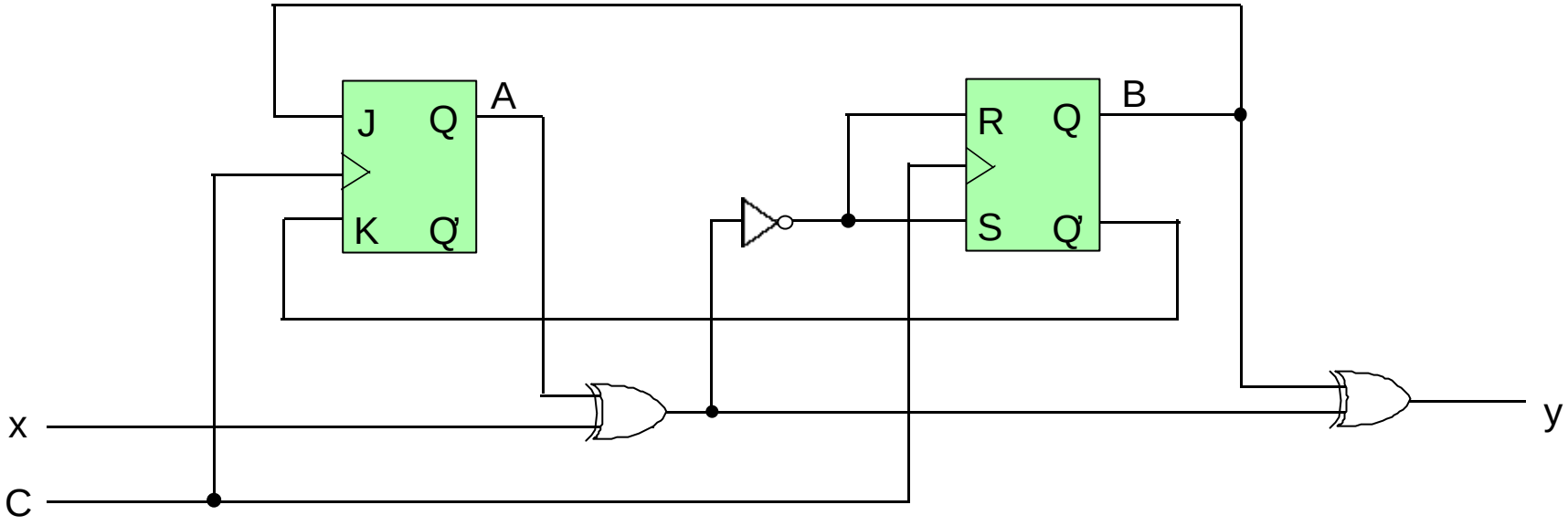
Sequential Circuit Analysis



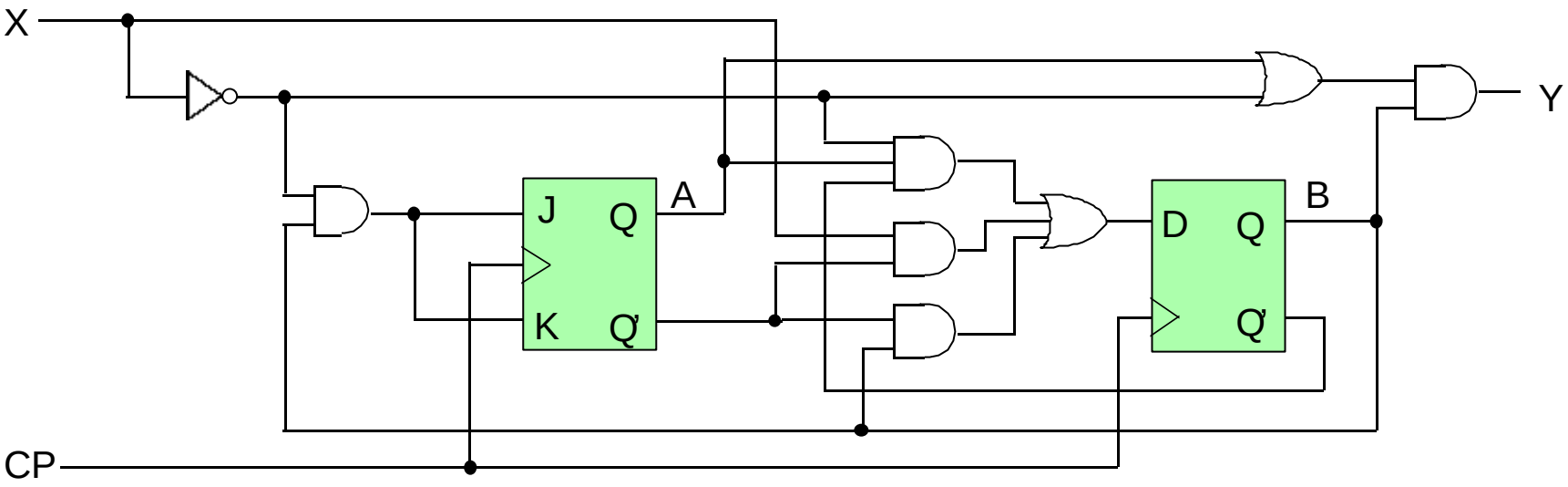
Sequential Circuit Analysis



Sequential Circuit Analysis



Sequential Circuit Analysis



- **출력방정식** : Y= (X' +A)B = X' B+AB
- Flip-flop **입력방정식** : J=K=X' B,
  D= X' AB' +XA' +A' B
- **상태방정식**
  A(t+1)= JA' +K' A = X' BA' +(X' B)' A
  = X' BA' +(X+B')A = X' BA' +XA+B' A
  B(t+1)= D= X' AB' +XA' +A' B

- **특성방정식**
  JK FF Q(t+1) = JQ' +K' Q
  D FF Q(t+1) = D

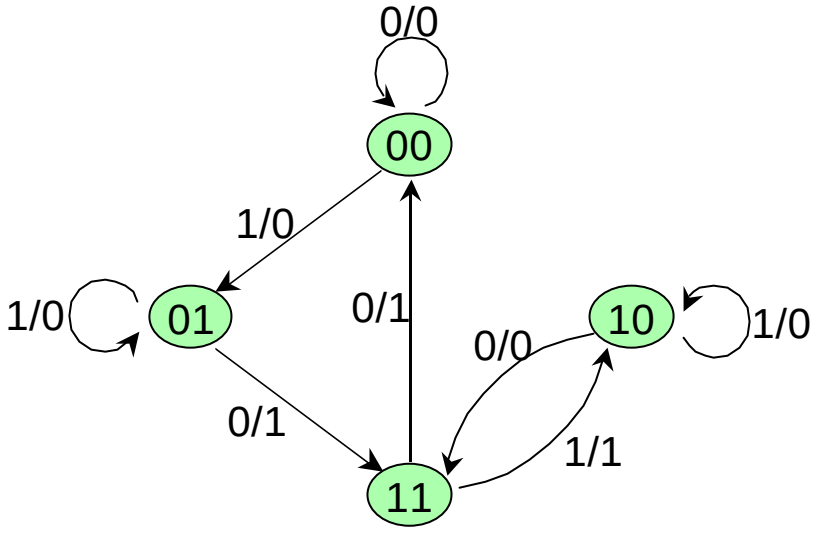
A \ Bx	00	01	11	10
0				1
1	1	1	1	

Sequential Circuit Analysis

◆ 상태표

현재 상태	다음상태		출력	
	x=0	x=1	x=0	x=1
A B	A B	A B	y	y
0 0	0 0	0 1	0	0
0 1	1 1	0 1	1	0
1 0	1 1	1 0	0	0
1 1	0 0	1 0	1	1

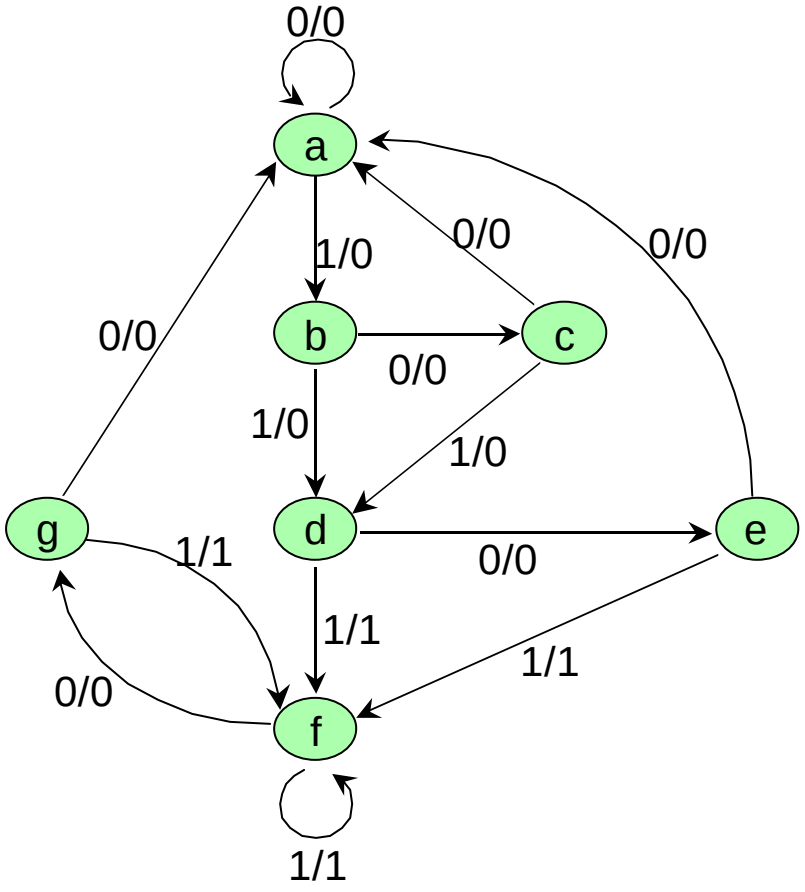
◆ 상태도



State Reduction

- 설계된 회로의 비용 : 게이트 수와 FF 수를 줄임으로서 비용감소 → 상태 수 줄임
- 상태 축소 : 입출력 요구조건을 변화시키지 않고 상태 수를 줄이는 절차

- 상태도



- 상태표

현재 상태	다음상태		출력	
	x=0	x=1	x=0	x=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

State Reduction

현재 상태	다음상태		출력	
	x=0	x=1	x=0	x=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

현재 상태	다음상태		출력	
	x=0	x=1	x=0	x=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	e	f	0	1

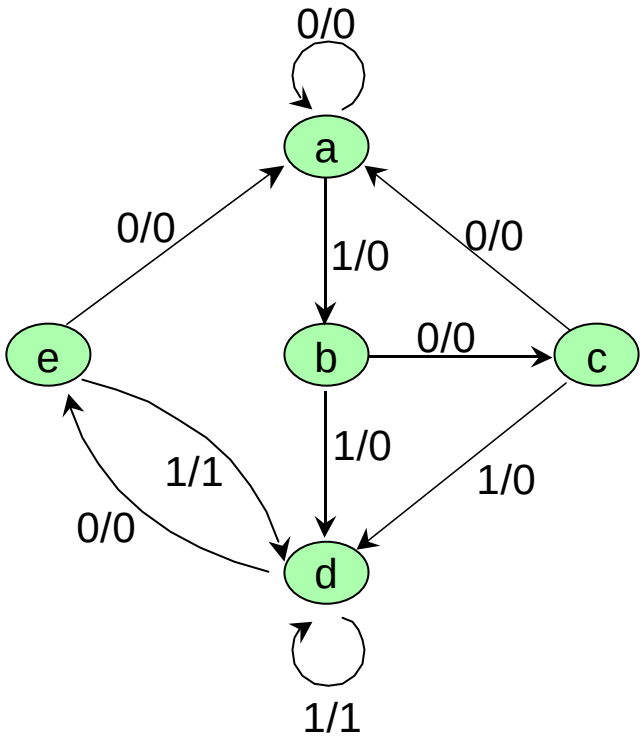
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	e	f	0	1

a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

State Reduction

◆ 간소화된 상태표 : 상태 2개가 축소되어 결과적으로 총 5개의 상태로 구성

현재 상태	다음상태		출력	
	x=0	x=1	x=0	x=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1



State Assignment

◆ 상태의 갯수가 5개이므로 2진수로 상태를 구분하기위해서는 최소 3bit 필요

◆ (상태할당1)

a=001, b=010, c=011, d=100, e=101

현재 상태	다음상태		출력	
	x=0	x=1	x=0	x=1
001	001	010	0	0
010	011	100	0	0
011	001	100	0	0
100	101	100	0	1
101	001	100	0	1

◆ (상태할당2)

a=000, b=010, c=011, d=101, e=111

현재 상태	다음상태		출력	
	x=0	x=1	x=0	x=1
000	000	010	0	0
010	011	101	0	0
011	000	101	0	0
101	111	101	0	1
111	000	101	0	1

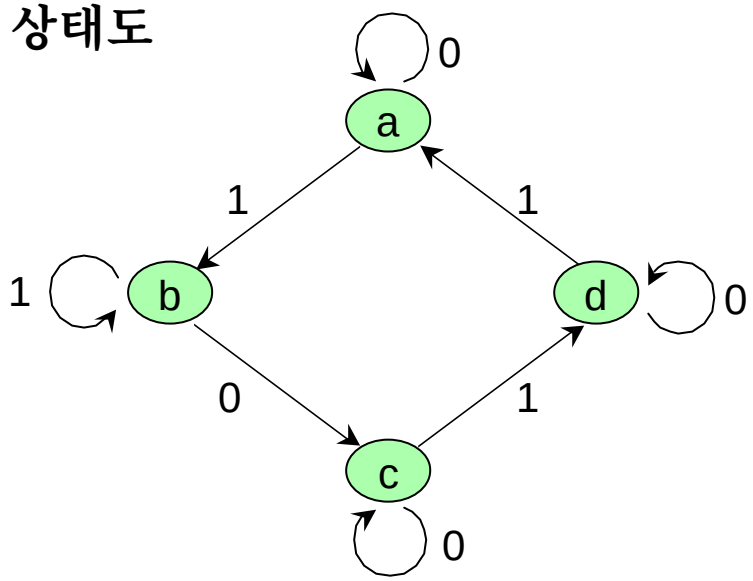
◆ 상태 할당 결과에 따라서 설계된 회로의 조합논리 부분의 복잡도가 달라진다

Sequential Circuit Design

- Design Procedure
  - (1) 회로의 동작 기술 - state diagram
  - (2) 회로에 관한 정보로 부터 state table 작성
  - (3) state reduction
  - (4) 상태표가 문자를 갖고 있으면 각 상태에 2진수 할당
  - (5) Flip-flop의 갯수를 결정하고 각각에 기호 부여
  - (6) Flip-flop의 type 결정
  - (7) state table로 부터 excitation table와 output table 작성
  - (8) 부울함수 간소화에 의해 output equation와 FF input equation 추출
  - (9) gate diagram
  - (10) design verification

Example of Sequential Circuit Design

① 상태도



② 상태표 작성

현재상태	다음상태	
	x=0	x=1
a	a	b
b	c	b
c	c	d
d	d	a

③ 상태축소
등가의 상태가 존재하지 않으므로
축소할 상태가 없다

④ 2진수 할당
a=00, b=01, c=10, d=11

현재상태	다음상태	
	x=0	x=1
00	00	01
01	10	01
10	10	11
11	11	00

Example of Sequential Circuit Design

⑤ FF의 갯수를 결정하고, 기호 부여
- 4개의 상태 존재→ 2개 FF 필요
- FF의 출력에 각각 A,B 할당

현재상태	다음상태	
	x=0	x=1
A B	A B	A B
0 0	0 0	0 1
0 1	1 0	0 1
1 0	1 0	1 1
1 1	1 1	0 0

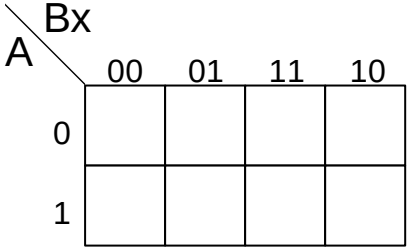
⑥ Flip-flop의 type 결정
- JK FF 사용

⑦ 상태표로 부터 여기표와 출력표 작성
- 출력 없음

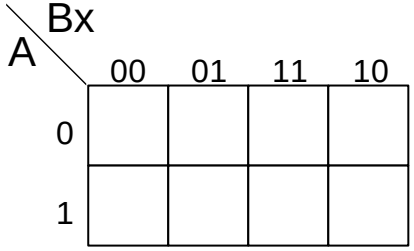
현재 상태	입력	다음 상태	FF 입력	
A B	x	A B	J_A K_A	J_B K_B
0 0	0			
0 0	1			
0 1	0			
0 1	1			
1 0	0			
1 0	1			
1 1	0			
1 1	1			

Example of Sequential Circuit Design

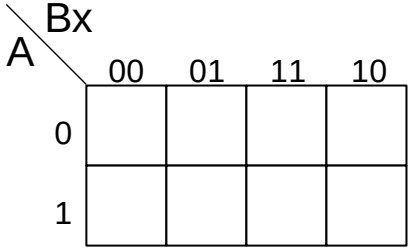
⑧ 부울함수 간소화에 의해 출력함수와 flip-flop의 입력함수 추출



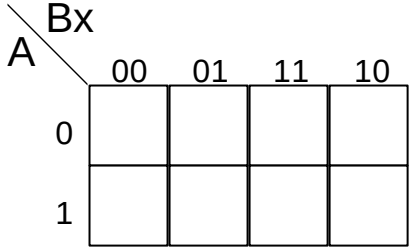
J_A=



K_A=

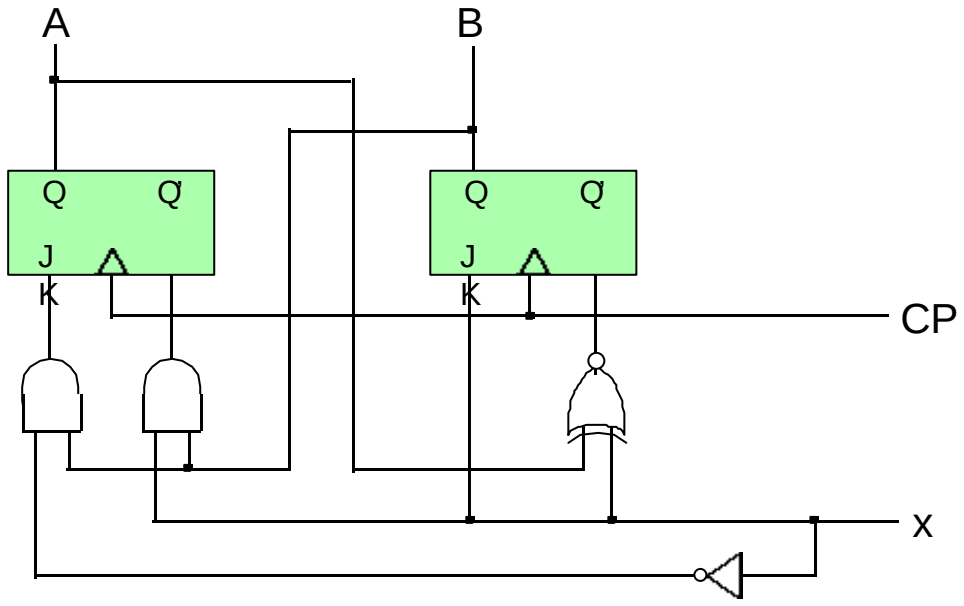


J_B=

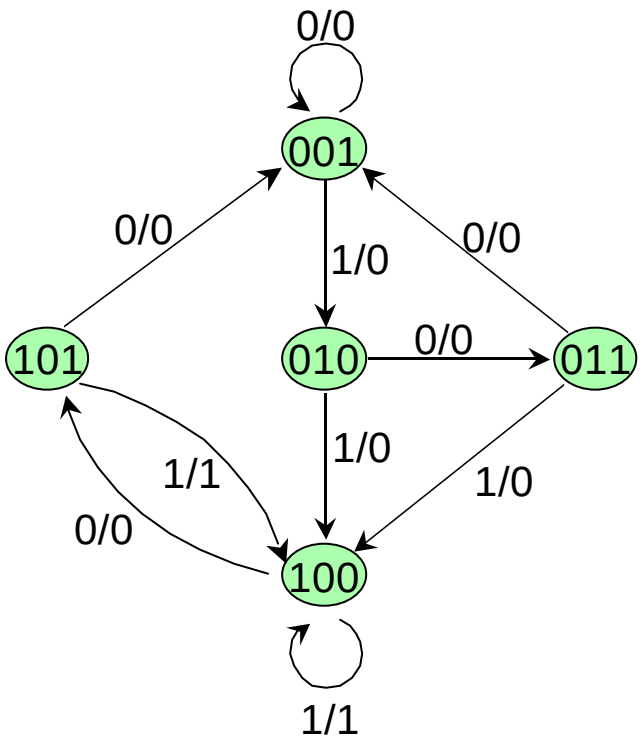


K_B=

⑨ 논리회로도



Sequential Circuit Design



현재 상태	입력	다음 상태	FF 입력			출력
A B C	x	A B C	R_A S_A	R_B S_B	R_C S_C	y
0 0 1	0	0 0 1	X 0	X 0	0 X	0
0 0 1	1	0 1 0	X 0	0 1	1 0	0
0 1 0	0	0 1 1	X 0	0 X	0 1	0
0 1 0	1	1 0 0	0 1	1 0	X 0	0
0 1 1	0	0 0 1	X 0	1 0	0 X	0
0 1 1	1	1 0 0	0 1	1 0	1 0	0
1 0 0	0	1 0 1	0 X	X 0	0 1	0
1 0 0	1	1 0 0	0 X	X 0	X 0	1
1 0 1	0	0 0 1	1 0	X 0	0 X	0
1 0 1	1	1 0 0	0 X	X 0	1 0	1

◆ 미사용상태 : 000, 110, 111

Sequential Circuit Design

AB \ Cx	00	01	11	10
00	X	X		
01				
11	X	X	X	X
10				

$R_A =$

AB \ Cx	00	01	11	10
00	X	X		
01				
11	X	X	X	X
10				

$R_B =$

AB \ Cx	00	01	11	10
00	X	X		
01				
11	X	X	X	X
10				

$R_C =$

AB \ Cx	00	01	11	10
00	X	X		
01				
11	X	X	X	X
10				

$Y =$

AB \ Cx	00	01	11	10
00	X	X		
01				
11	X	X	X	X
10				

$S_A =$

AB \ Cx	00	01	11	10
00	X	X		
01				
11	X	X	X	X
10				

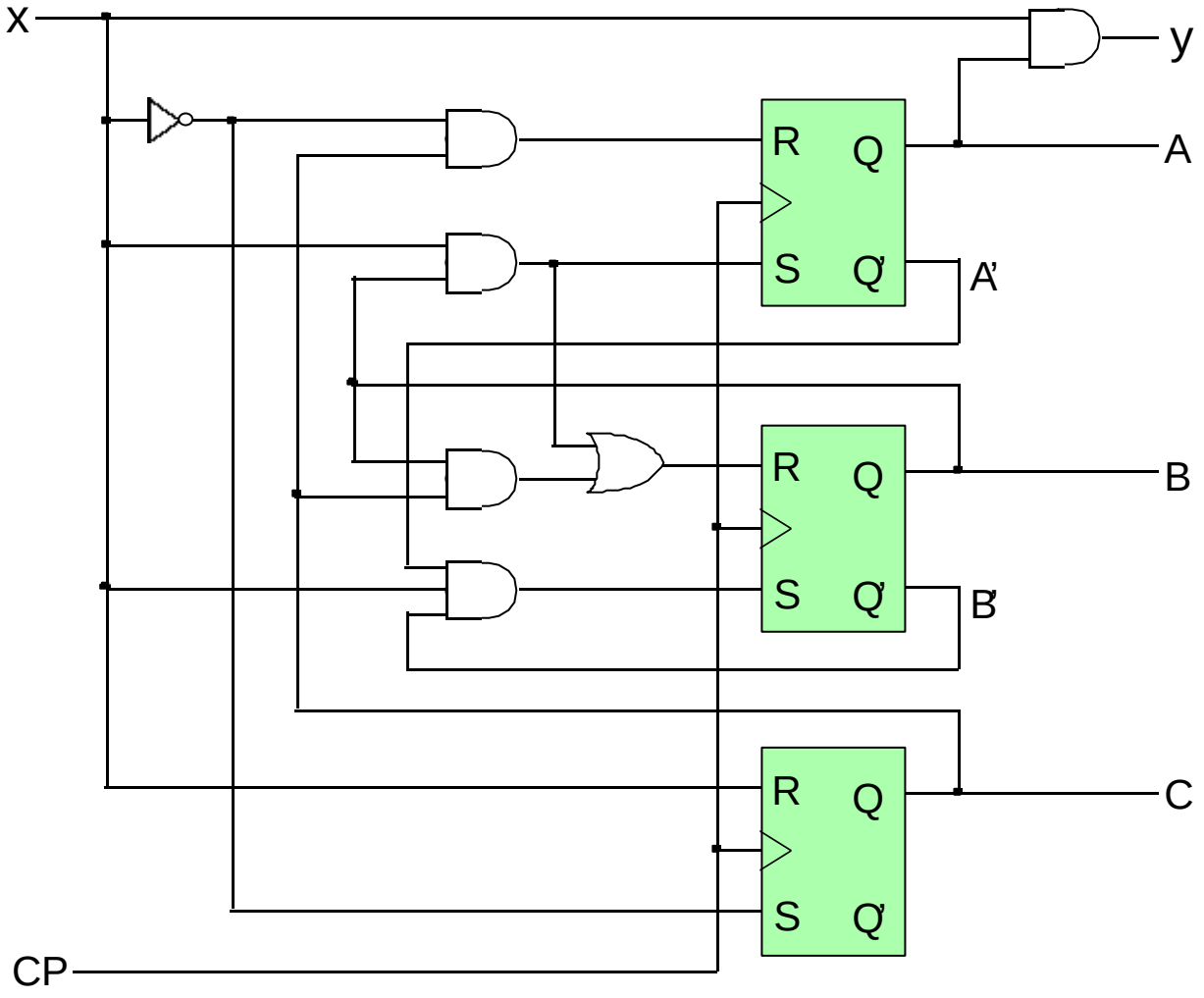
$R_B =$

AB \ Cx	00	01	11	10
00	X	X		
01				
11	X	X	X	X
10				

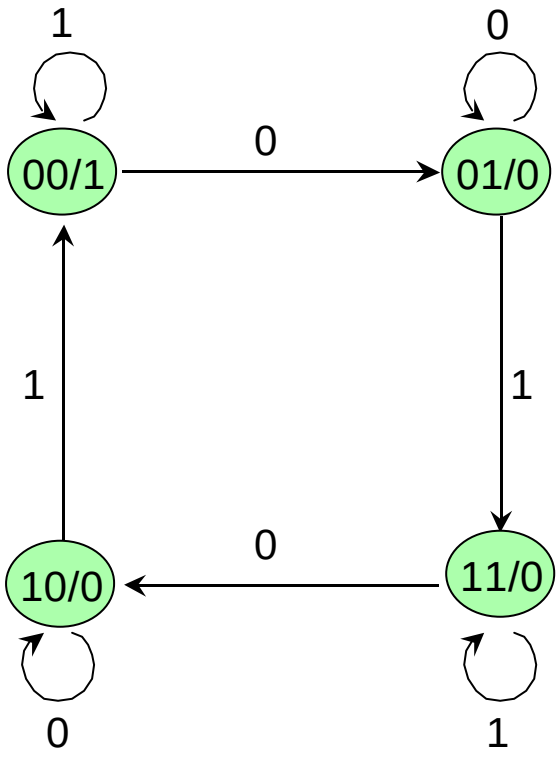
$R_C =$

Sequential Circuit Design

◆ 논리회로도

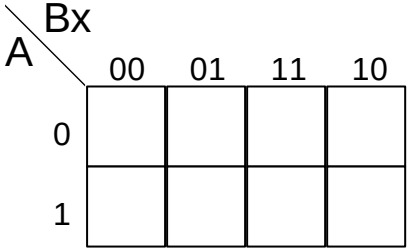


Sequential Circuit Design

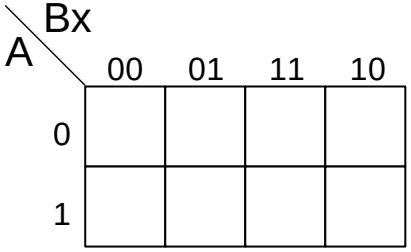


현재 상태	입력	다음 상태	FF 입력	
A B	x	A B	J_A K_A	J_B K_B
0 0	0	0 1	0 X	1 X
0 0	1	0 0	0 X	0 X
0 1	0	0 1	0 X	X 0
0 1	1	1 1	1 X	X 0
1 0	0	1 0	X 1	0 X
1 0	1	0 0	X 1	0 X
1 1	0	1 0	X 0	X 1
1 1	1	1 1	X 0	X 0

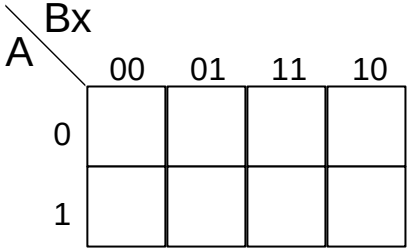
Sequential Circuit Design



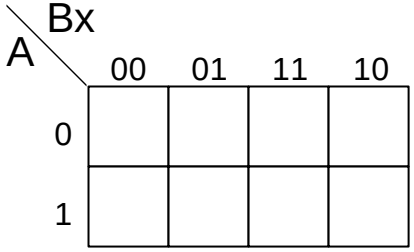
$J_A = BX$



$K_A = B'$



$J_B = A'X'$



$K_B = AX'$