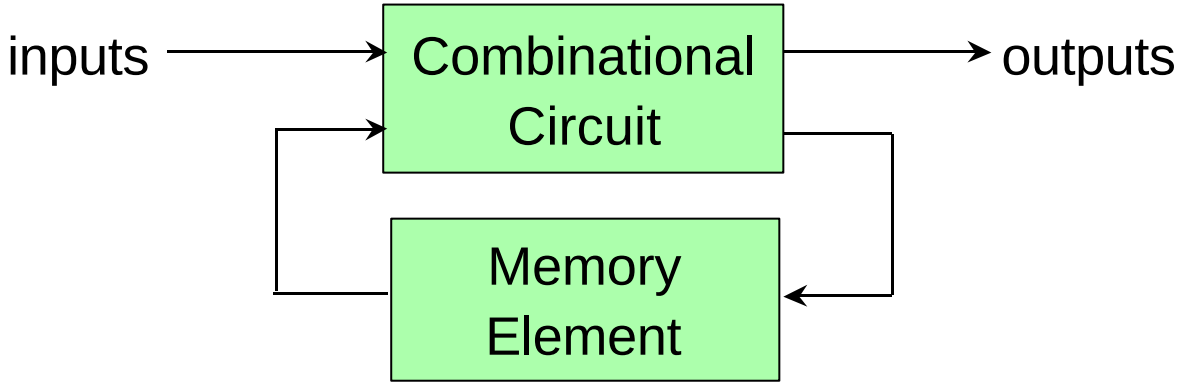
6장 Sequential Logic Circuit

Sequential Logic Circuit (順序論理回路)

- 출력 = f(현재입력, 현재상태) : 현재 입력, 현재 상태가 출력에 영향
- 현재상태가 기억요소에 저장된후 다시 입력으로 feedback되어 출력에 영향

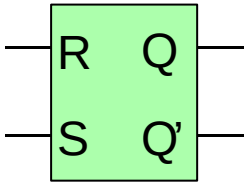


- Synchronous sequential logic circuit (同期式順序回路)
  - 클럭발생기에 의해서 발생되는 클럭펄스가 들어오는 시점에서 회로가 동기화되어 동작
- Asynchronous sequential logic circuit(非同期式順序回路)
  - 동기신호없이 입력신호 또는 내부신호가 변경되는 순서에 따라서 동작

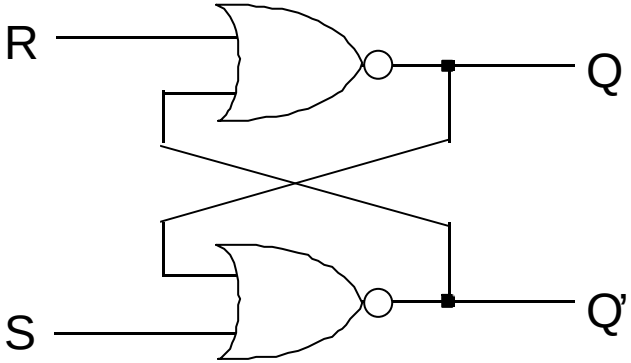
Flip-Flop

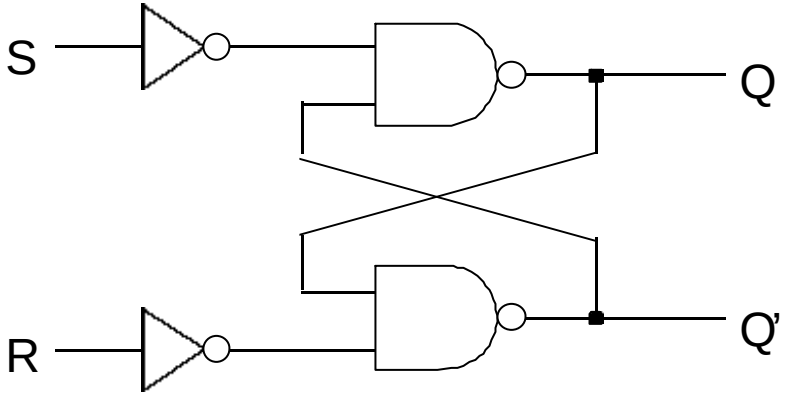
- 입력이 변경되기 전까지 안정된 상태를 유지하는 메모리소자
- 1 bit의 정보를 저장할 수 있는 binary cell

(1) RS flip-flop



① 게이트 회로도 (gate diagram)





RS Flip-Flop

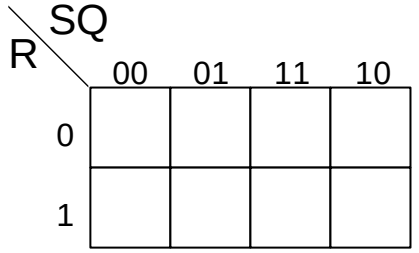
② 특성표(characteristic table)

R	S	Q(t+1)
0	0	
0	1	
1	0	
1	1	

③ 변형된 특성표

R	S	Q(t)	Q(t+1)
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

④ 특성방정식(characteristic equation)



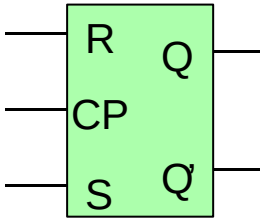
Q(t+1)=

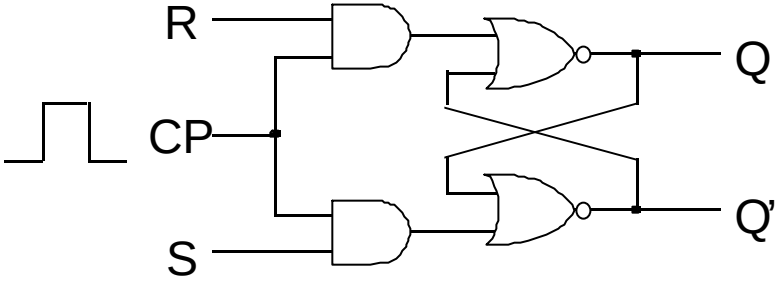
⑤ 여기표(excitation table)

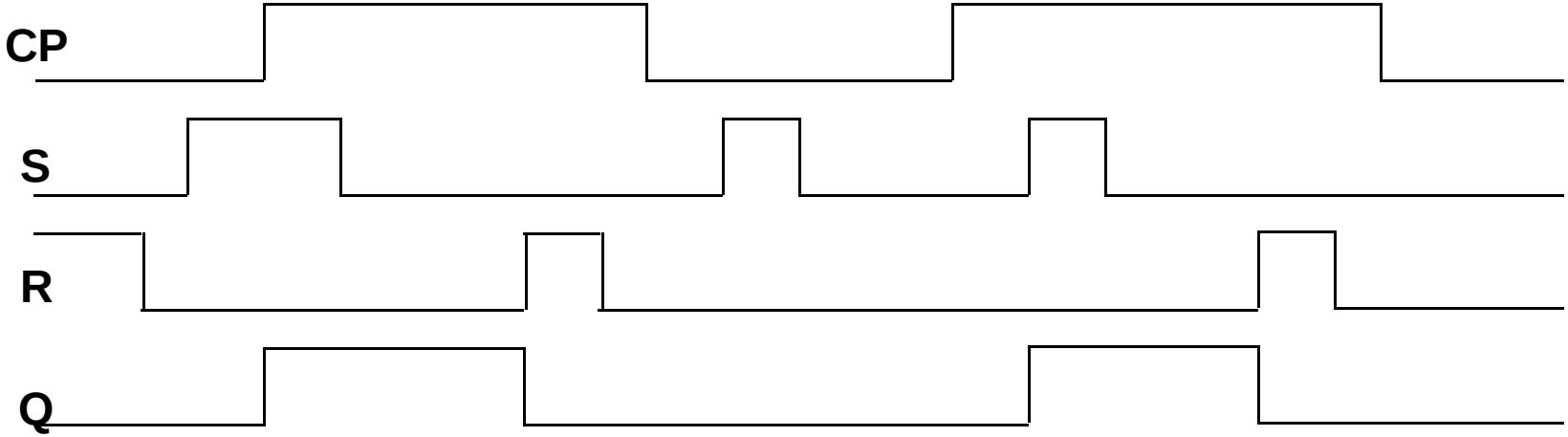
Q(t)	Q(t+1)	R	S
0	0		
0	1		
1	0		
1	1		

Clocked RS Flip-Flop

- 제어입력(CP)이 추가
  - CP=0 이면 Q, Q' 는 불변 (No change !!)
  - CP=1 이면 Q는 R, S에 따라서 결정



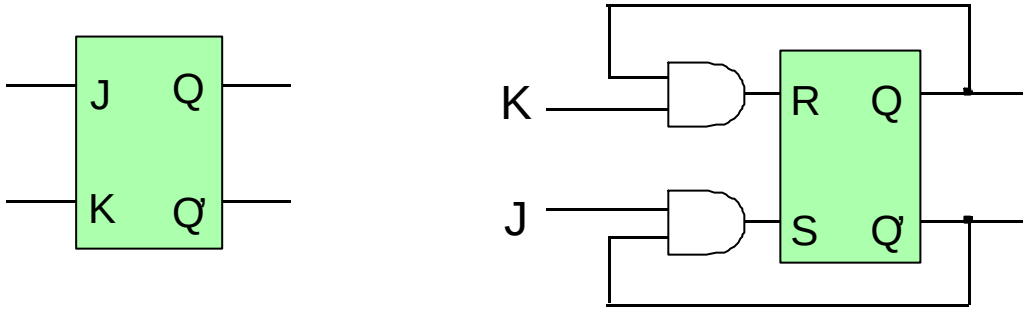




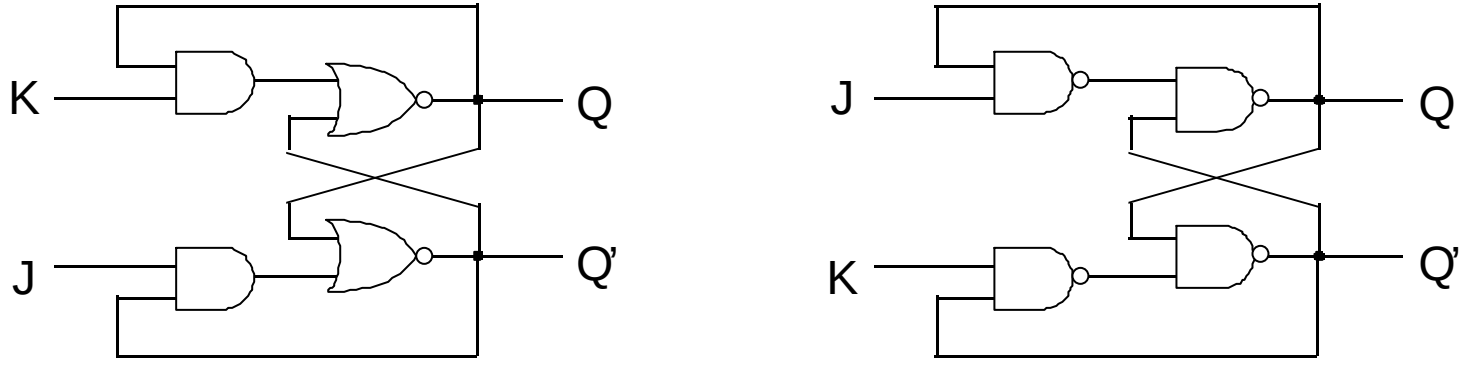
JK Flip-Flop

(2) JK flip-flop

◆ RS flip-flop**의 부정상태를 사용할 수 있도록 개선**



① **게이트 회로도** (gate diagram)



JK Flip-Flop

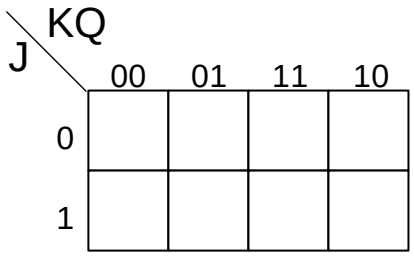
② 특성표(characteristic table)

J	K	Q(t+1)
0	0	
0	1	
1	0	
1	1	

③ 변형된 특성표

J	K	Q(t)	Q(t+1)
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

④ 특성방정식(characteristic equation)



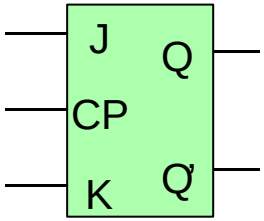
Q(t+1)=

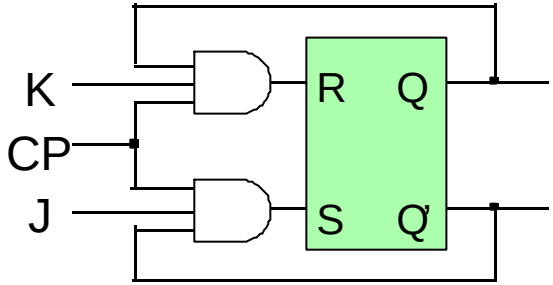
⑤ 여기표(excitation table)

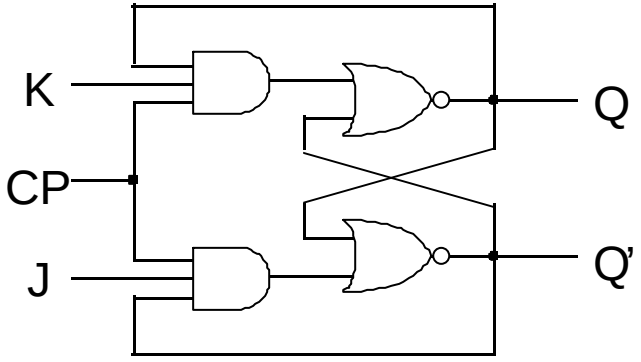
Q(t)	Q(t+1)	J	K
0	0		
0	1		
1	0		
1	1		

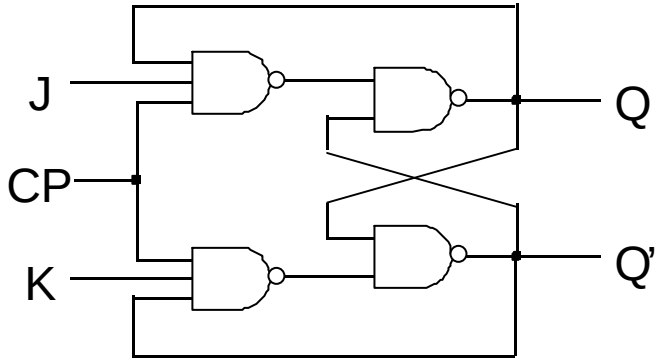
Clocked JK Flip-Flop

- 제어입력(CP)이 추가
  - CP=0 이면 Q, Q' 는 불변 (No change !!)
  - CP=1 이면 Q는 J, K에 따라서 결정

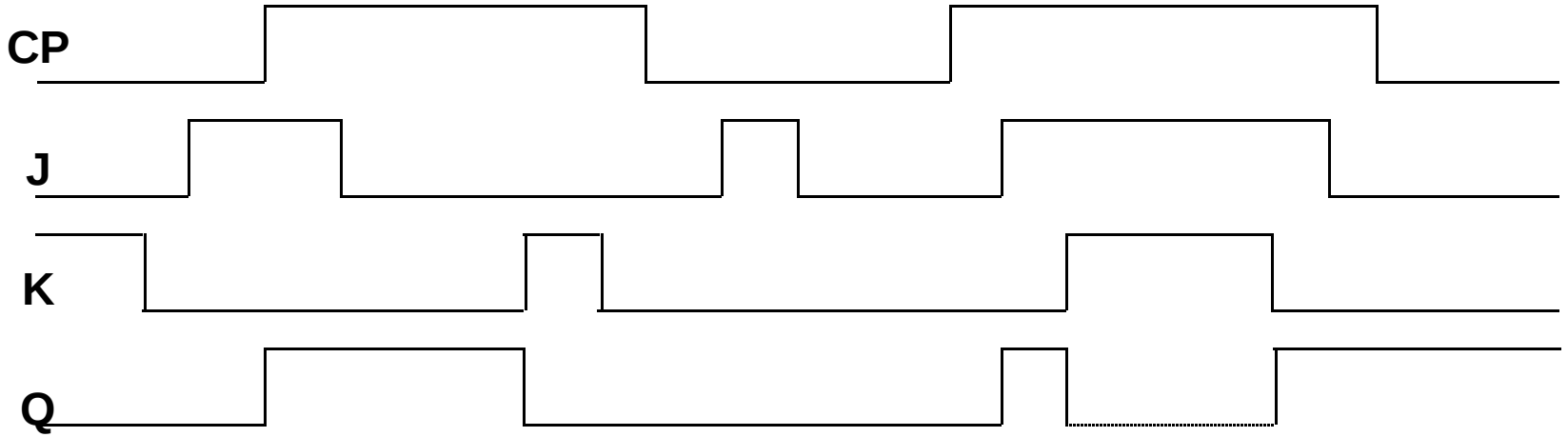








Clocked JK Flip-Flop

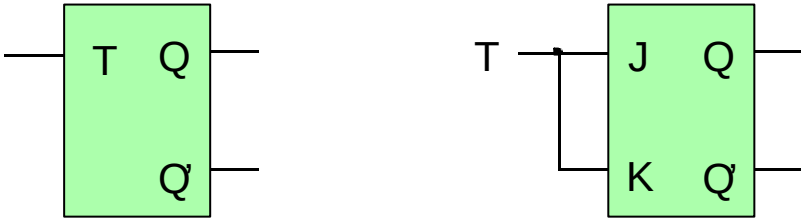


- CP=J=K=1 **이면** Q, Q' **는 계속적으로 반전**
  따라서 『 CP**의 유지시간 <** FF**의 전파지연시간 』의 조건을 만족해야 함**
- **해결방법**
  - Master-slave flip-flop
  - Edge-triggered flip-flop

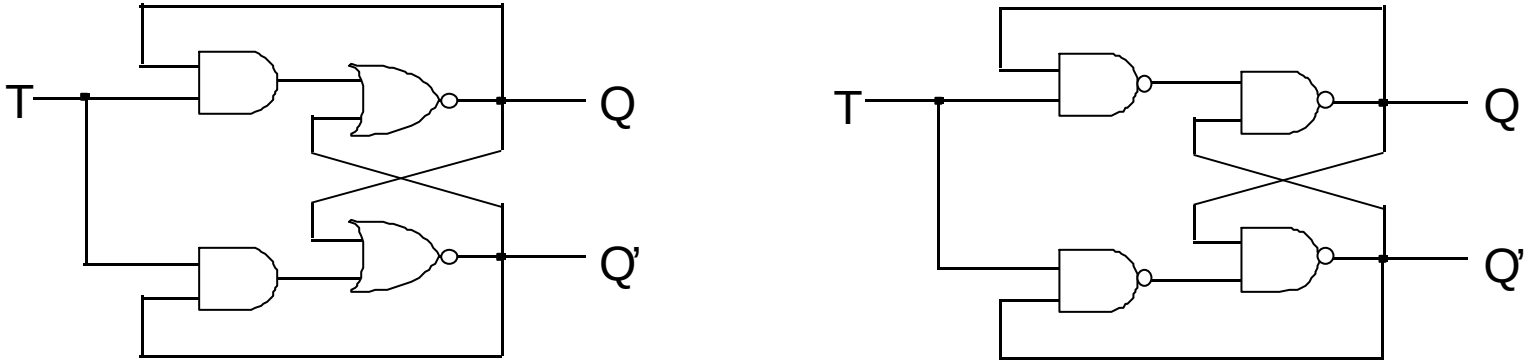
T Flip-Flop

(3) T flip-flop

◆ JK flip-flop의 J,K단자를 하나로 묶어서 구성



① 게이트 회로도 (gate diagram)

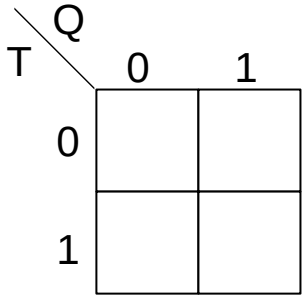


T Flip-Flop

② 특성표(characteristic table)

T	Q(t+1)
0	
1	

④ 특성방정식(characteristic equation)



Q(t+1)=

③ 변형된 특성표

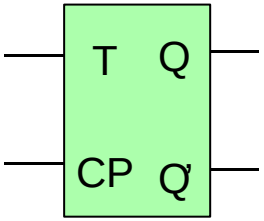
T	Q(t)	Q(t+1)
0	0	
0	1	
1	0	
1	1	

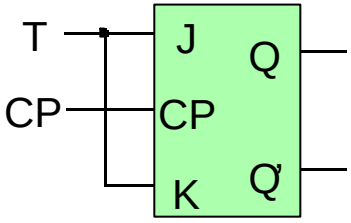
⑤ 여기표(excitation table)

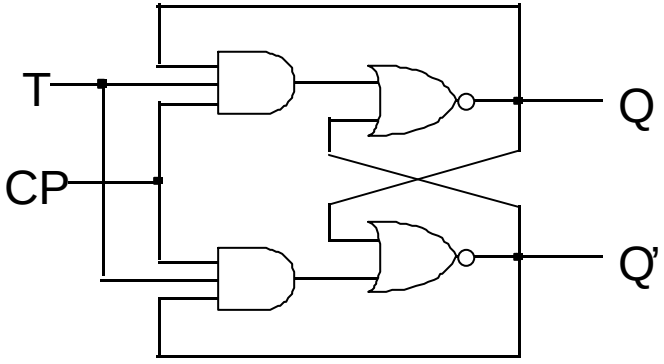
Q(t)	Q(t+1)	T
0	0	
0	1	
1	0	
1	1	

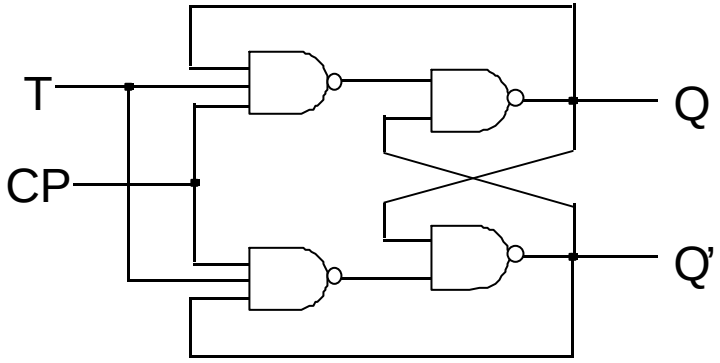
Clocked T Flip-Flop

- 제어입력(CP)이 추가
  - CP=0 이면 Q, Q' 는 불변 (No change !!)
  - CP=1 이면 Q는 J, K에 따라서 결정

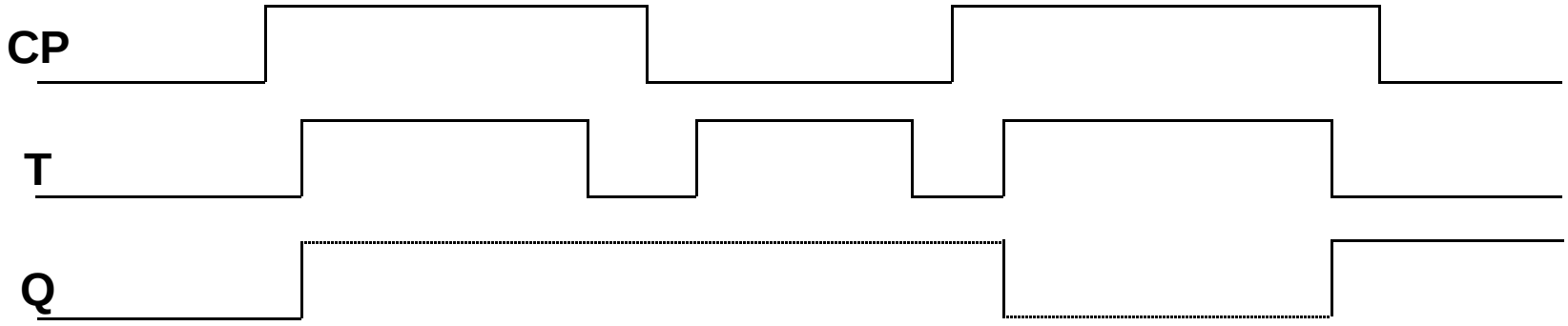








Clocked T Flip-Flop

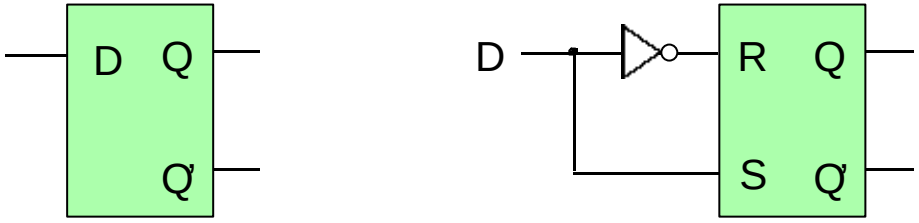


- CP=T=1 **이면** Q, Q' **는 계속적으로 반전**
  따라서 『 CP**의 유지시간 <** FF**의 전파지연시간 』의 조건을 만족해야 함**
- **해결방법**
  - Master-slave flip-flop
  - Edge-triggered flip-flop

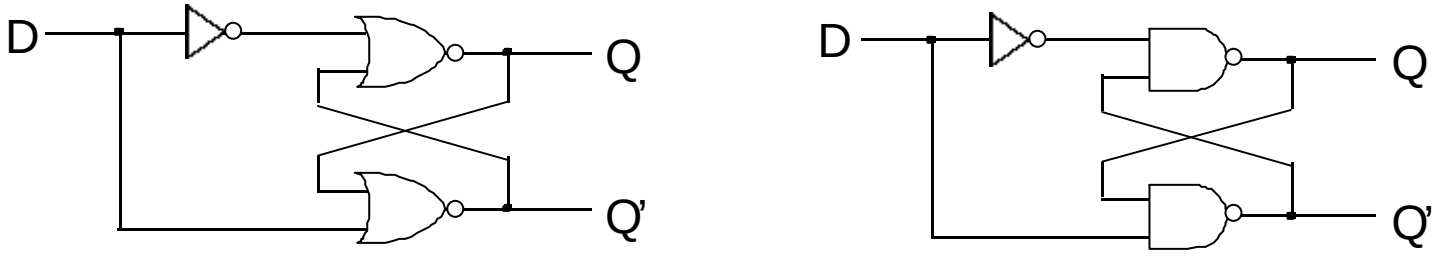
D Flip-Flop

(4) D flip-flop

◆ RS flip-flop의 R,S단자에 서로 다른 입력을 인가



① 게이트 회로도 (gate diagram)

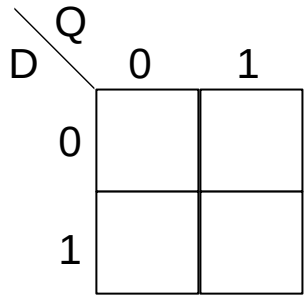


D Flip-Flop

② 특성표(characteristic table)

D	Q(t+1)
0	
1	

④ 특성방정식(characteristic equation)



Q(t+1)=

③ 변형된 특성표

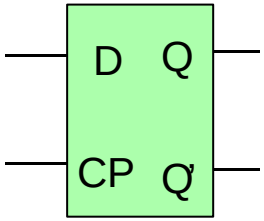
D	Q(t)	Q(t+1)
0	0	
0	1	
1	0	
1	1	

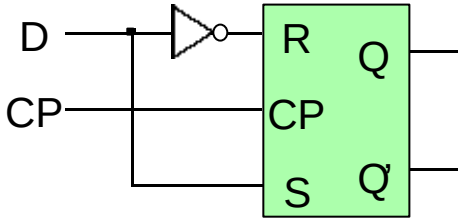
⑤ 여기표(excitation table)

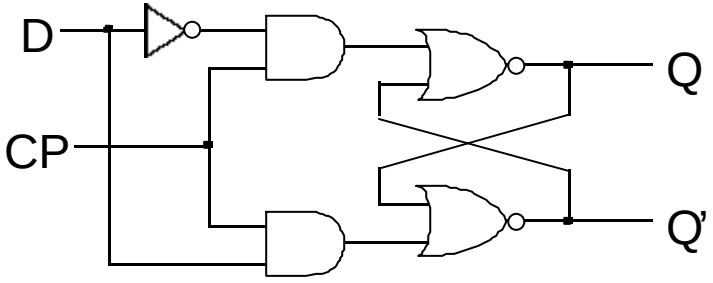
Q(t)	Q(t+1)	D
0	0	
0	1	
1	0	
1	1	

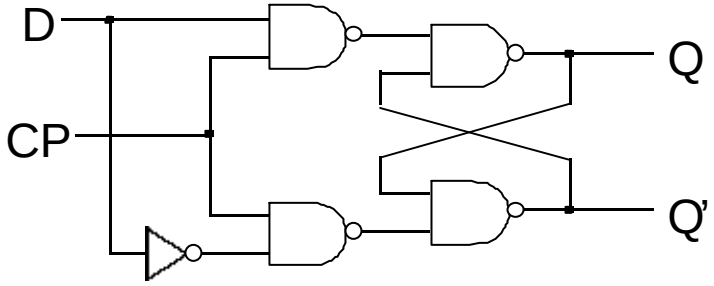
Clocked D Flip-Flop

- 제어입력(CP)이 추가
  - CP=0 이면 Q, Q' 는 불변 (No change !!)
  - CP=1 이면 Q는 D에 따라서 결정





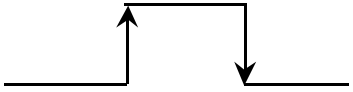




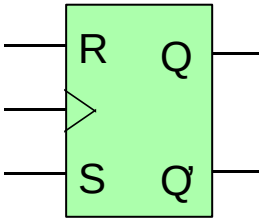
Flip-Flop의 Triggering

- Triggering : **입력신호의 변화가 FF의 상태를 순간적으로 변화시킴**
  - Level triggering : 0 **또는** 1**의 상태에서** FF**의 상태천이**
  - Edge triggering : positive edge **또는** negative edge**에서** FF**의 상태천이**

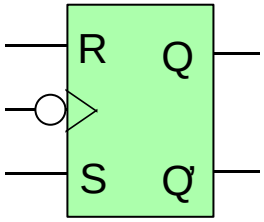
- Positive edge and negative edge



- Positive edge triggered RS FF

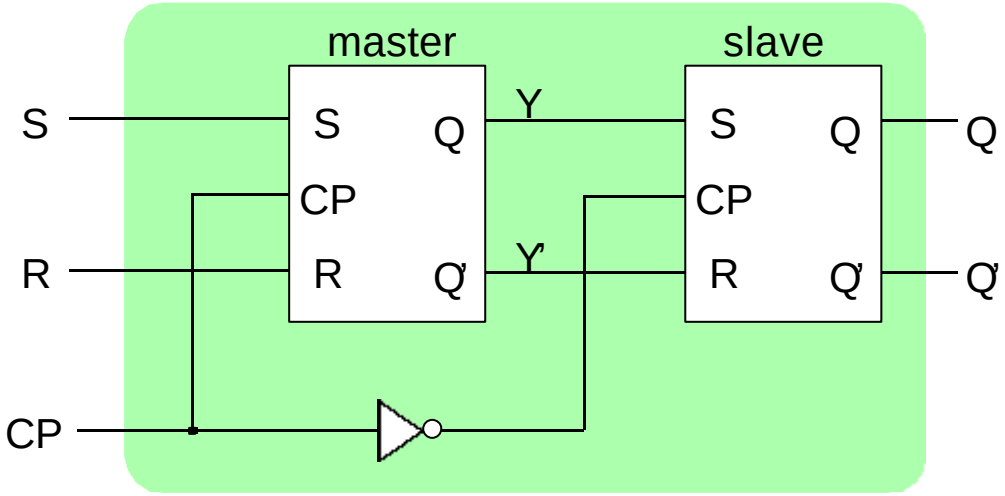


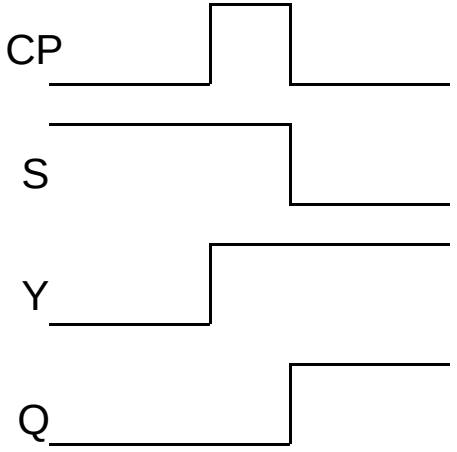
- Negative edge triggered RS FF



Master-Slave Flip-Flop

- CP가 0→1 이면 master flip-flop 동작
  R, S에 따라서 Y, Y' 가 결정
- CP가 1→0 이면 slave filp-flop 동작
  Y, Y' 에 따라서 Q, Q' 가 결정
- 즉, CP의 negative edge에서 출력 Q가 나타남



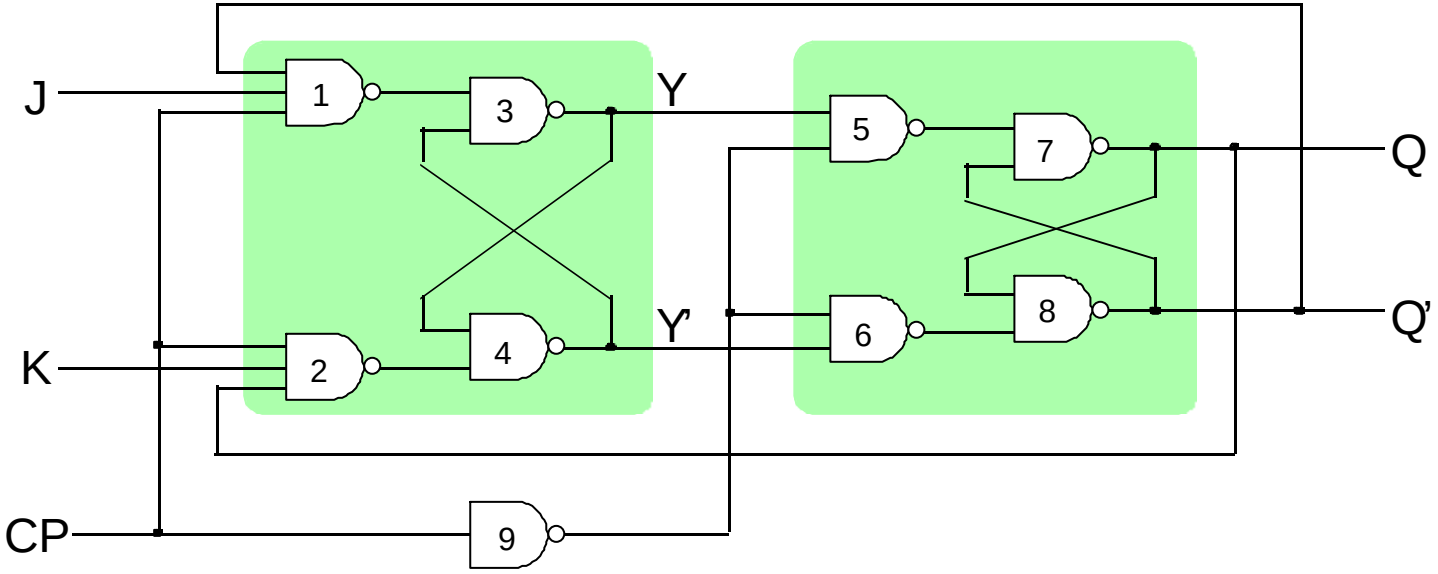


Clocked Master-Slave JK Flip-Flop

- Master flip-flop : NAND gate 1, 2, 3, 4

  Slave filp-flop : NAND gate 5, 6, 7, 8
- CP가 0→1 이면 master flip-flop 동작, J, K에 따라서 Y, Y' 가 결정

  CP가 1→0 이면 slave filp-flop 동작, Y, Y' 에 따라서 Q, Q' 가 결정
- 즉, CP의 negative edge에서 출력 Q가 나타남

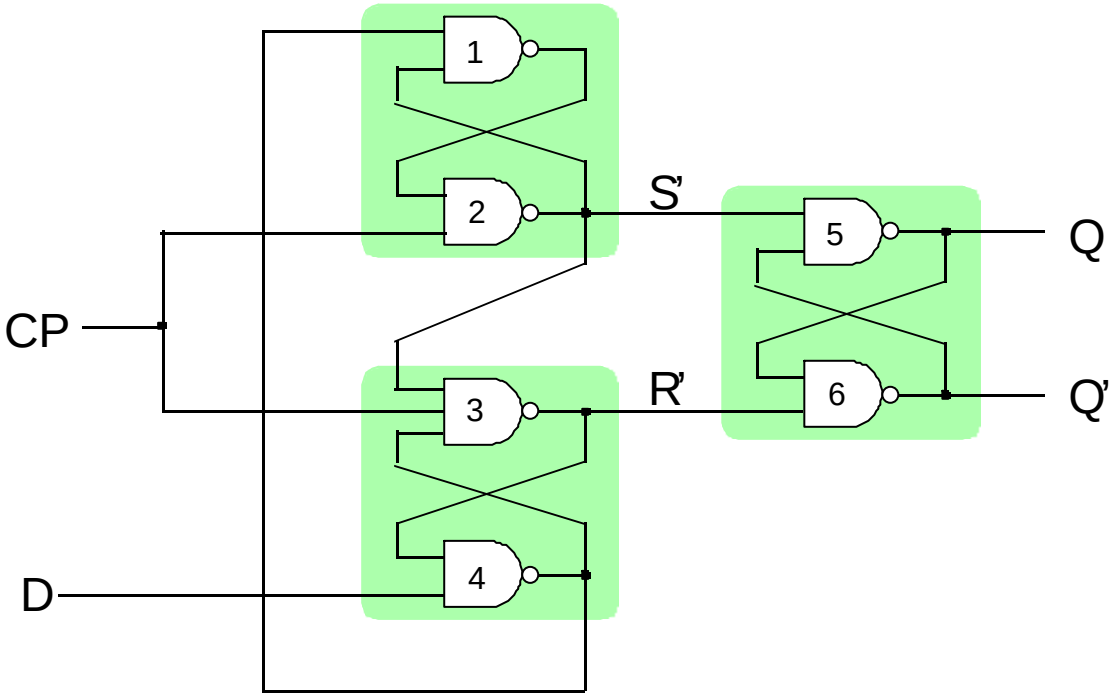


Edge-Triggered Flip-Flop

- ◆ 클럭신호의 edge에서만 FF의 상태 변화가 일어나도록 동기시킨 FF

❑ Positive edge triggered D FF

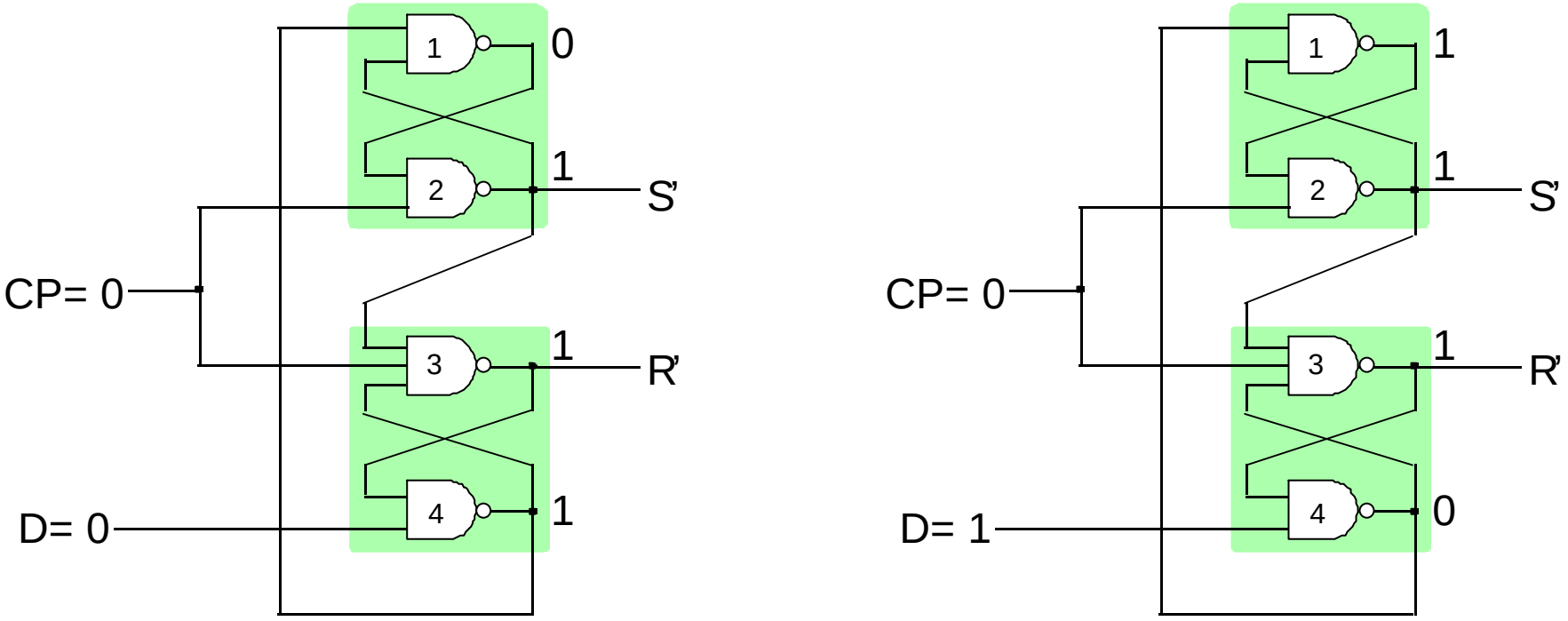
- ◆ Negative edge, level-0, level-1에서는 출력이 변화하지 않고, positive edge에서만 D값이 출력에 전달된다
- ◆ 3개의 RS FF으로 구성



S'	R'	S	R	Q
0	0	1	1	
0	1	1	0	
1	0	0	1	
1	1	0	0	

Edge-Triggered D Flip-Flop

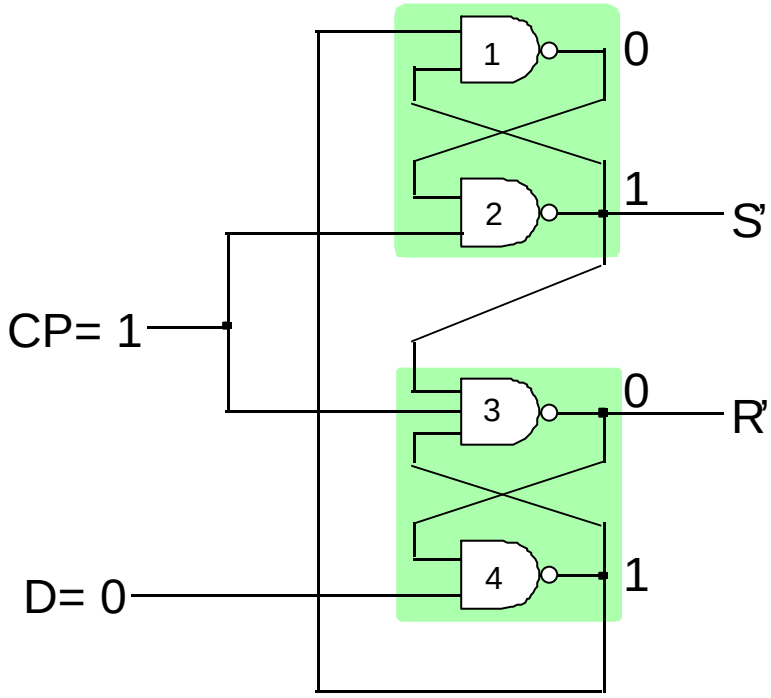
❑ CP=0 인 경우

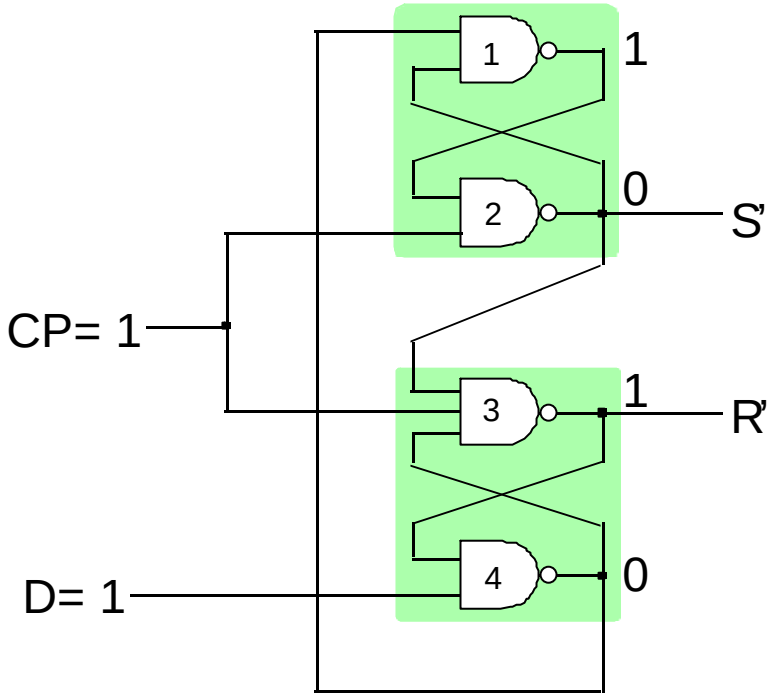


- CP=0 일때는 R=S=0 이므로 입력에 관계없이 출력은 변화없음 (현재상태 유지)
- setup time
  - 클럭펄스가 인가되기 전에 D입력이 일정한 값을 유지해야 하는 최소의 시간
  - D 값이 변하면 NAND4와 NAND1의 출력이 변하므로, NAND4와 NAND1의 값이 안정된 값을 갖기전까지는 D값이 변경되서는 안된다
  - 즉, NAND4로부터 NAND1까지 지나는데 걸리는 전달지연시간

Edge-Triggered D Flip-Flop

❑ CP=1 인 경우





• CP=1 && D=0 ⇒ S=0, R=1 ⇒ Q=0

• CP=1 && D=1 ⇒ S=1, R=0 ⇒ Q=1

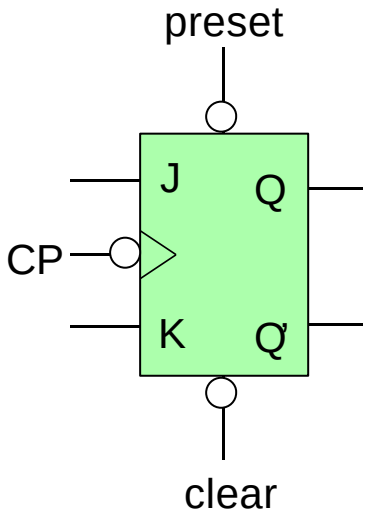
• hold time

- 클럭펄스의 positive edge가 인가된후, D값이 변하지 않아야 하는 시간
- 즉, NAND3의 지연시간 : D값에 무관하게 NAND1, NAND4의 출력을 그대로 유지하기위해 R값은 0이 된다

Direct Input

◆ CP에 의해서 동기되지 않고, 직접 입력에 의해 FF을 초기화

- preset or set : 출력을 1로 초기화
- reset or clear : 출력을 0로 초기화



입 력					출 력	
clear	preset	CP	J	K	Q	Q'
0	1	X	X	X	0	1
1	0	X	X	X	1	0
1	1	↓	0	0	No change	
1	1	↓	0	1	0	1
1	1	↓	1	0	1	0
1	1	↓	1	1	Toggle	