5장 MSI와 LSI를 이용한 조합논리회로

5.1 서론

5.2 2진병렬가산기

5.3 10진가산기

5.4 크기비교기

5.5 Decoder

5.6 Multiplexer

5.7 ROM

5.8 PLA

5.9 결론

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MSI & PLD

- MSI (Medium Scale Integrate Circuit)
  - 하나의 칩에 수십개의 gate를 구현한 집적회로
  - adder, subtractor, comparator, decoder, encoder, multiplexer, demultiplexer, ROM, PLA

- PLD (programmable logic device)
  - 프로그램 가능한 fuse(스위치)로 연결된 게이트의 array로 구성된 IC
  - AND - OR array로 구성 → sum of product 실현
  - 초기상태는 모든 fuse가 연결되어 있어, fuse를 끊음으로써 프로그램
  - PLD는 AND-OR array에서 fuse의 배치 형태에 따라 PROM, PLA, PAL로 나뉨

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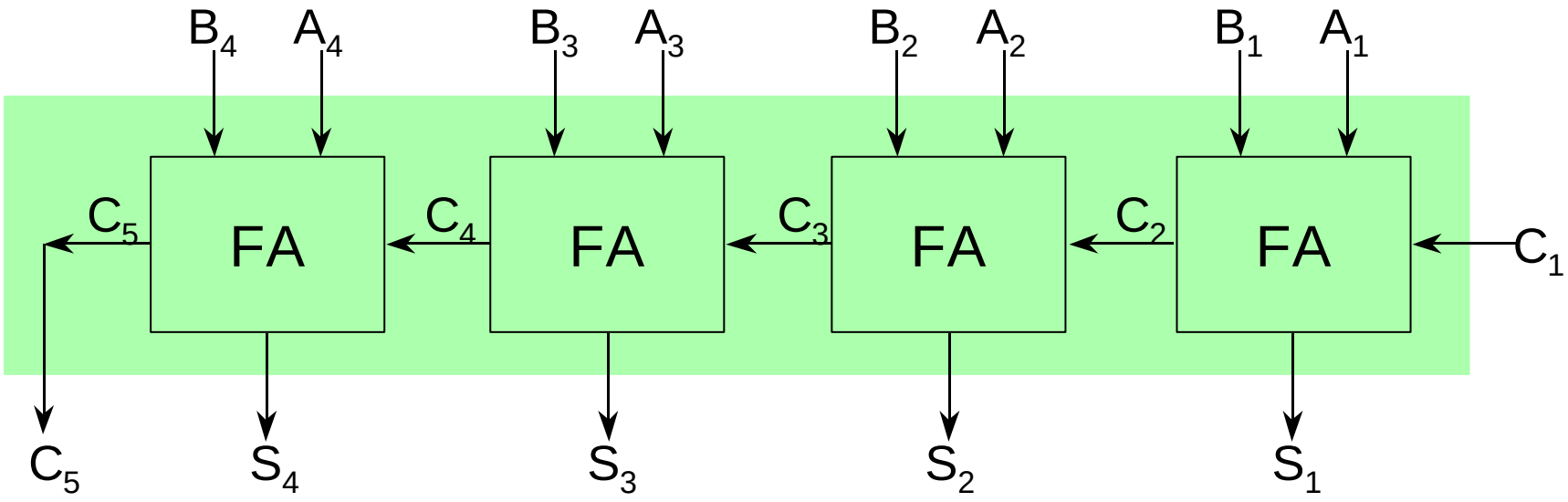
Binary Parallel Adder(Binary Ripple Carry Adder)

- 4-bit binary parallel adder

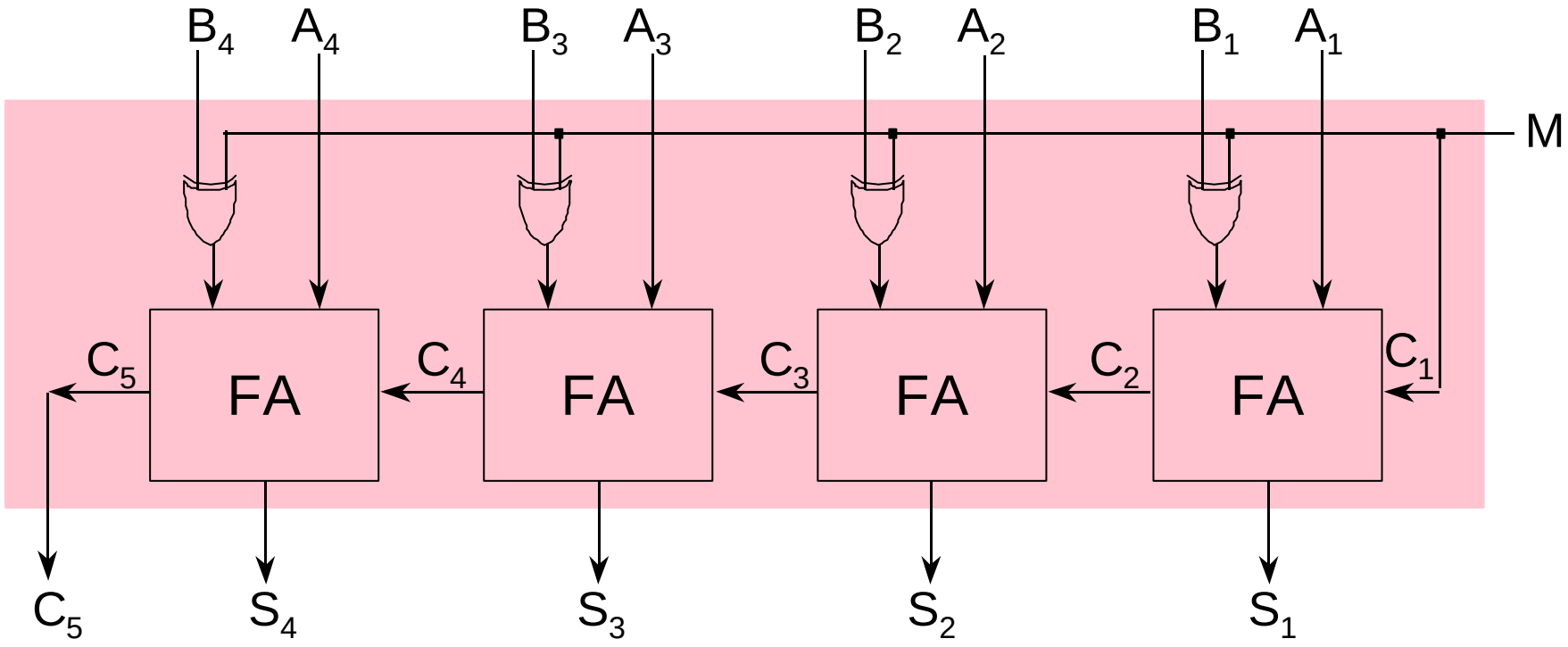
$$\begin{array}{rr} & B_4\,B_3\,B_2\,B_1 \\ + & A_4\,A_3\,A_2\,A_1 \\ \hline & S_4\,S_3\,S_2\,S_1 \\ C_5\,C_4\,C_3\,C_2 & C_1 \end{array}$$

$$\begin{array}{rr} & 1011 \\ + & 1001 \\ \hline & 10100 \end{array}$$



Binary Adder-Subtractor

- 4-bit binary adder-subtractor
  - If M=0, then A+B
  - If M=1, then A+(B에대한 1의보수)+1 = A+(B에대한 2의보수) = A - B



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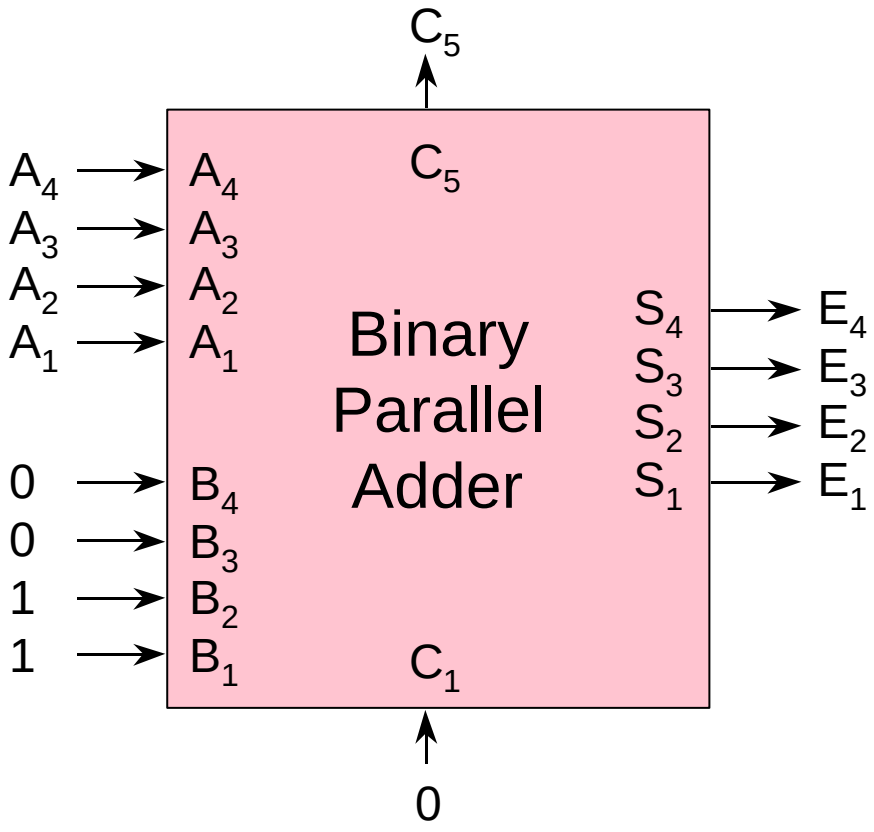
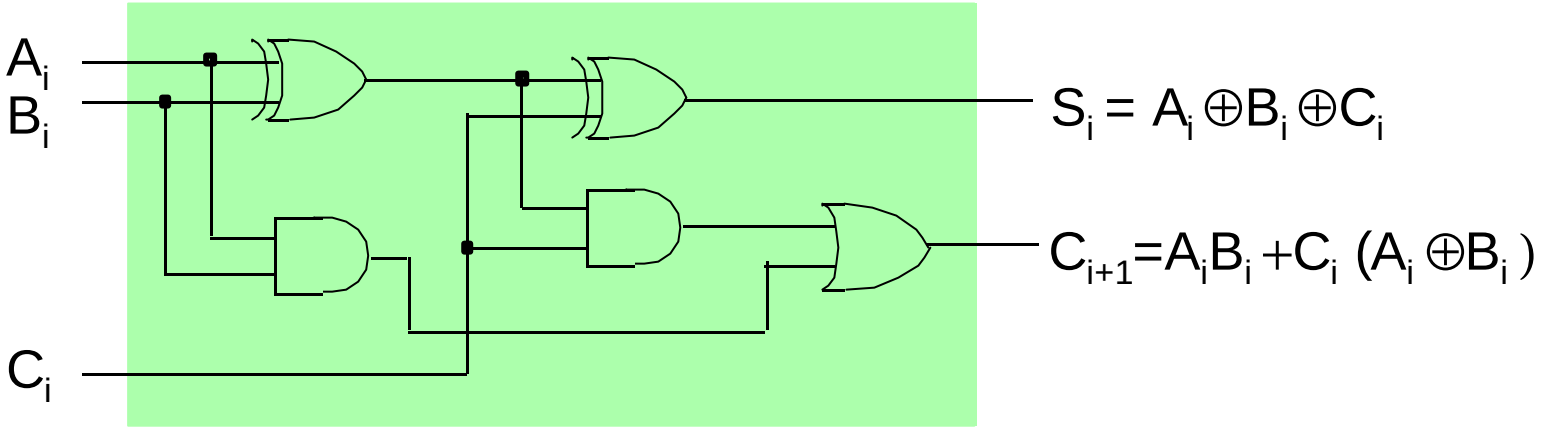
MSI를 이용한 설계

- BCD to Excess-3 code converter
  - $A_4A_3A_2A_1 + 0011 = E_4E_3E_2E_1$
    (BCD) (Excess-3)



Carry Propagation

- n bit의 병렬가산 → 입력은 동시에 인가되지만 전단의 캐리가 전달되어야만 합을 계산
- 전가산기



- Pi와 Gi를 정의
  - $P_i = A_i \oplus B_i$, $G_i = A_i \cdot B_i \Rightarrow S_i = P_i \oplus C_i$, $C_{i+1} = G_i + P_i C_i$
  - $C_2 = G_1 + P_1C_1$

    $C_3 = G_2 + P_2C_2 = G_2 + P_2(G_1+P_1C_1) = G_2+P_2G_1+P_2P_1C_1$

    $C_4 = G_3 + P_3C_3 = G_3 + P_3(G_2+P_2G_1+P_2P_1C_1) = G_3+P_3G_2+P_3P_2G_1+P_3P_2P_1C_1$
  - C_i 는 C_{i-1}을 기다릴 필요가 없으므로, S_2,S_3,S_4는 동일한 지연시간을 갖는다

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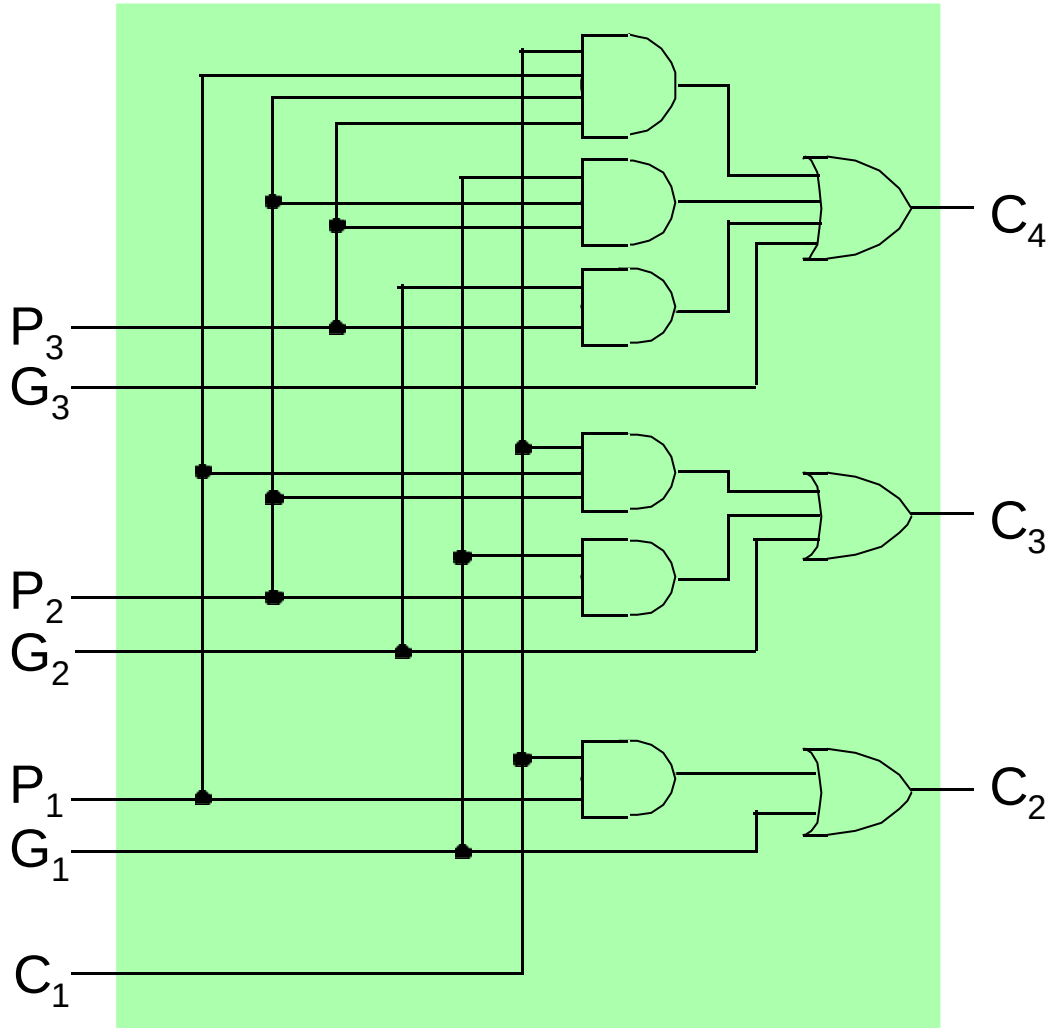
Look-Ahead Carry Generator의 회로도

- C_{i+1}을 계산하기위해 C_i를 기다리지 않아도 된다



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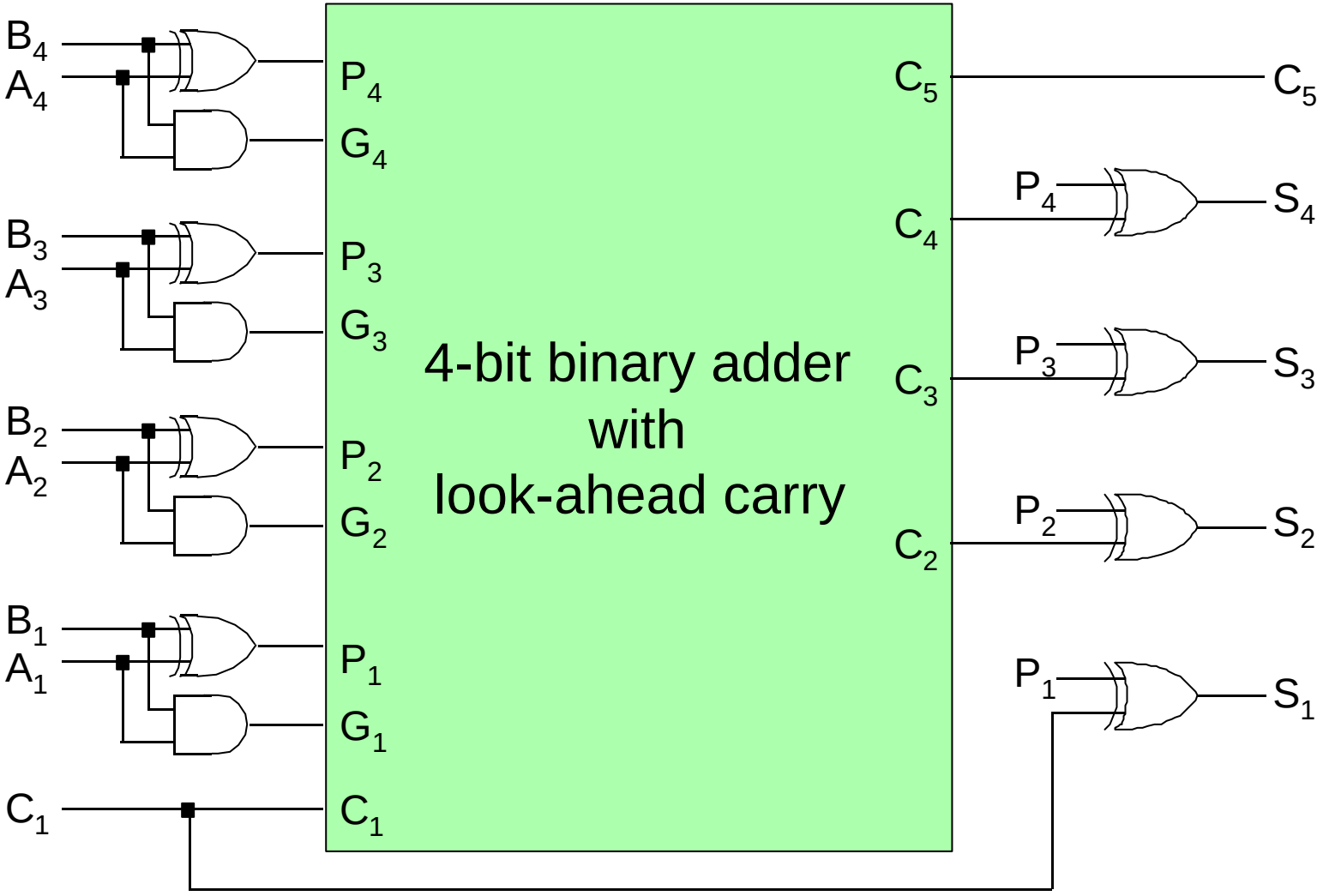
4-bit Binary Adder with Look-Ahead Carry



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BCD Adder

◆ (0+0) ≤ BCD합 ≤ (9+9+1)

십진	이진수 합					BCD 합				
	K	Z_8	Z_4	Z_2	Z_1	C	S_8	S_4	S_2	S_1
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	1
2	0	0	0	1	0	0	0	0	1	0
3	0	0	0	1	1	0	0	0	1	1
4	0	0	1	0	0	0	0	1	0	0
5	0	0	1	0	1	0	0	1	0	1
6	0	0	1	1	0	0	0	1	1	0
7	0	0	1	1	1	0	0	1	1	1
8	0	1	0	0	0	0	1	0	0	0
9	0	1	0	0	1	0	1	0	0	1

십진	이진수 합					BCD 합				
	K	Z_8	Z_4	Z_2	Z_1	C	S_8	S_4	S_2	S_1
10	0	1	0	1	0	1	0	0	0	0
11	0	1	0	1	1	1	0	0	0	1
12	0	1	1	0	0	1	0	0	1	0
13	0	1	1	0	1	1	0	0	1	1
14	0	1	1	1	0	1	0	1	0	0
15	0	1	1	1	1	1	0	1	0	1
16	1	0	0	0	0	1	0	1	1	0
17	1	0	0	0	1	1	0	1	1	1
18	1	0	0	1	0	1	1	0	0	0
19	1	0	0	1	1	1	1	0	0	1

◆ 0 ↔ 9 : **이진수 합** = BCD 합

◆ 10 ↔ 19 : **이진수 합** + 0110 = BCD 합

① K=1 ② Z_8Z_4 = 11 ③ Z_8Z_2 = 11

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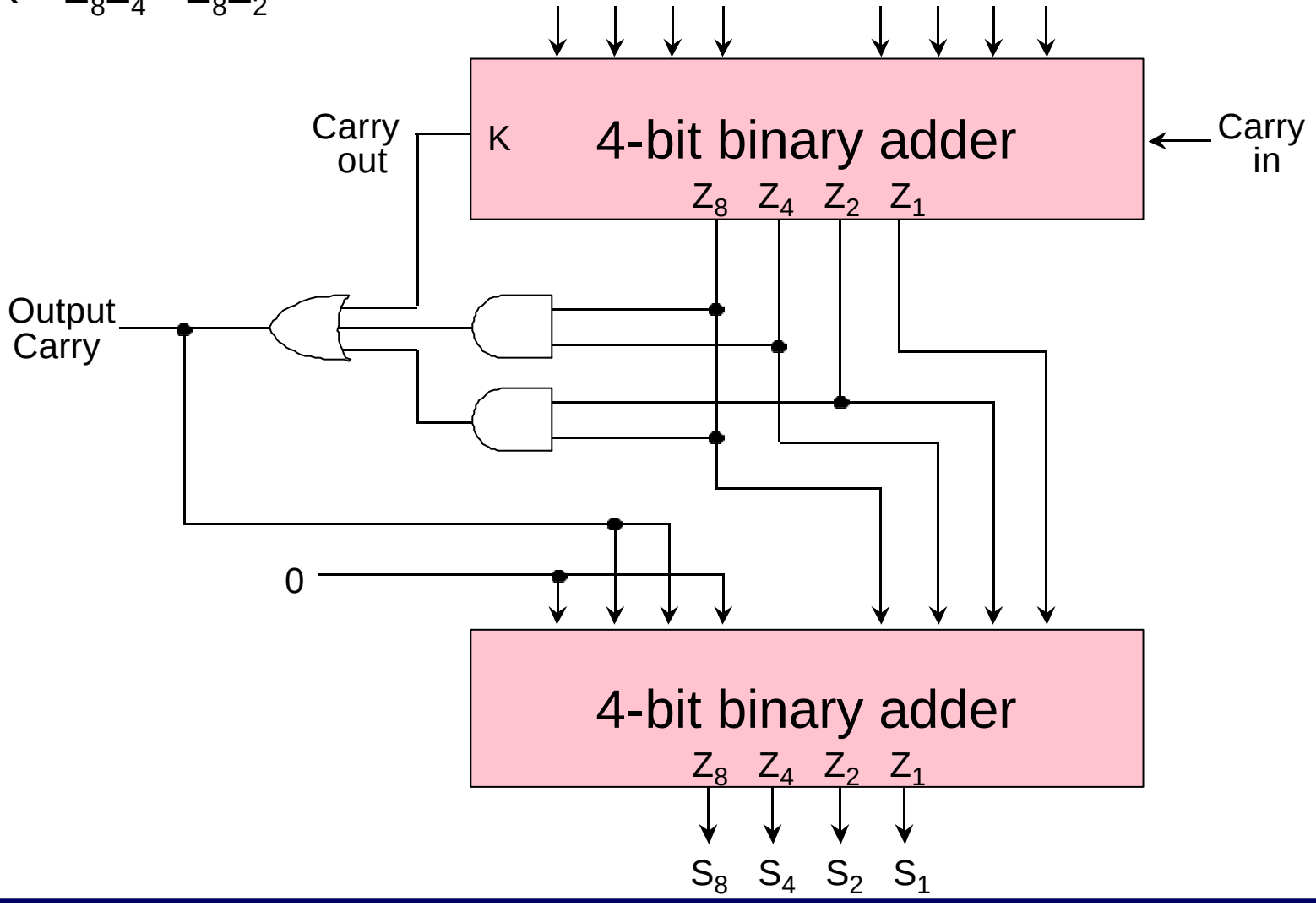
BCD Adder의 회로도

- $C = K + Z_8Z_4 + Z_8Z_2$



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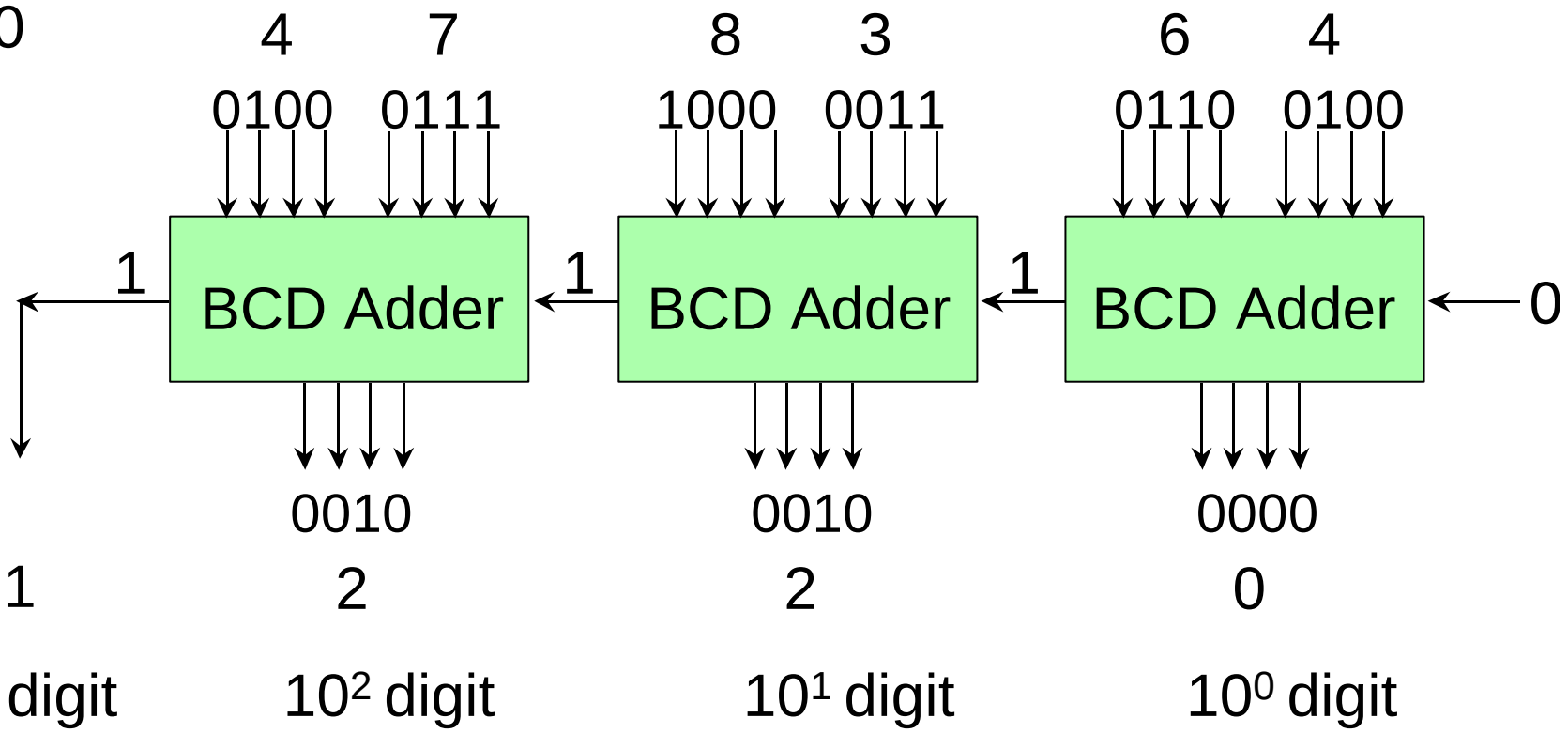
BCD Adder

```
  486
+ 734
------
 1220
```



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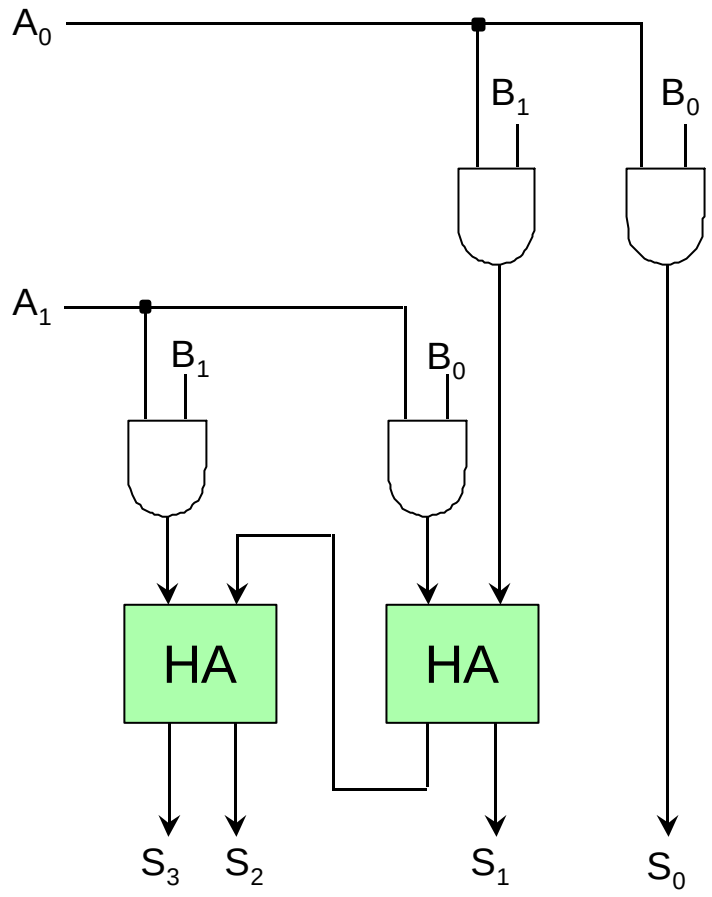
Binary Multiplier Design (2bitx2bit)

- B_1B_0 X A_1A_0의 계산

$$
\begin{array}{cccc}
 & & B_1 & B_0 \\
 & X & A_1 & A_0 \\
\hline
 & & A_0B_1 & A_0B_0 \\
 & A_1B_1 & A_1B_0 & \\
\hline
S_3 & S_2 & S_1 & S_0
\end{array}
$$

$$
\begin{array}{cccc}
 & & 1 & 0 \\
 & X & 1 & 1 \\
\hline
 & & 1 & 0 \\
 & 1 & 0 & \\
\hline
 & 1 & 1 & 0
\end{array}
$$



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Binary Multiplier Design (4bitx3bit)

- $B_3B_2B_1B_0$ X A_2 A_1A_0의 계산

			B_3	B_2	B_1	B_0
		X		A_2	A_1	A_0
			A_0B_3	A_0B_2	A_0B_1	A_0B_0
		A_1B_3	A_1B_2	A_1B_1	A_1B_0	
	A_2B_3	A_2B_2	A_2B_1	A_2B_0		
S_6	S_5	S_4	S_3	S_2	S_1	S_0

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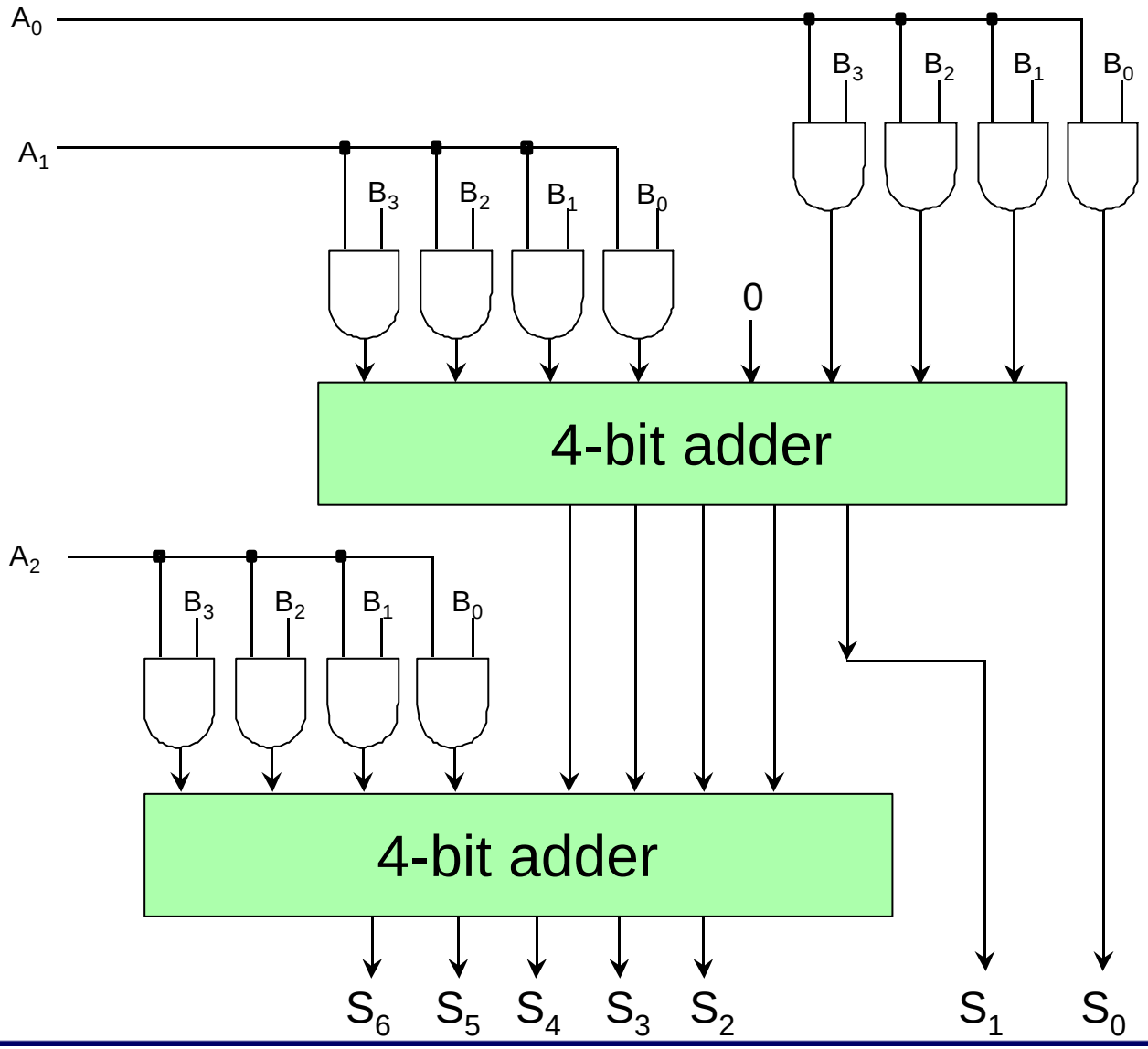
4bitx3bit Multiplier의 회로도



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Binary Multiplier Design (4bitx4bit)

- $B_3B_2B_1B_0$ X $A_3A_2A_1A_0$의 계산

				B_3	B_2	B_1	B_0
				X A_3	A_2	A_1	A_0
				A_0B_3	A_0B_2	A_0B_1	A_0B_0
			A_1B_3	A_1B_2	A_1B_1	A_1B_0	
		A_2B_3	A_2B_2	A_2B_1	A_2B_0		
	A_3B_3	A_3B_2	A_3B_1	A_3B_0			
S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

- 일반적으로 K bit x M bit 의 경우
  - (K x M)개의 AND gate
  - (M-1)개의 K-bit adder
  - (K+M) bit의 결과

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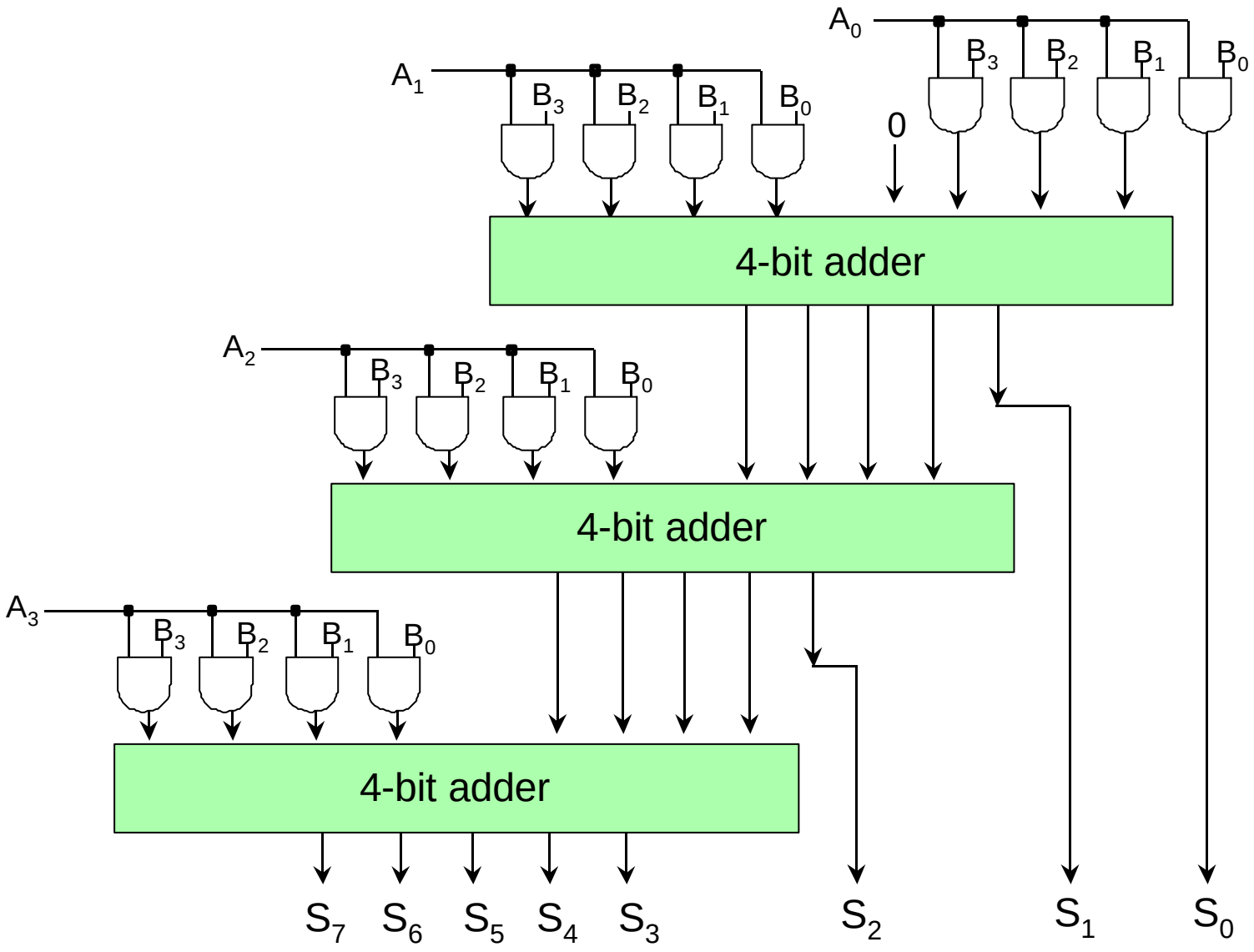
4bitx4bit Multiplier의 회로도



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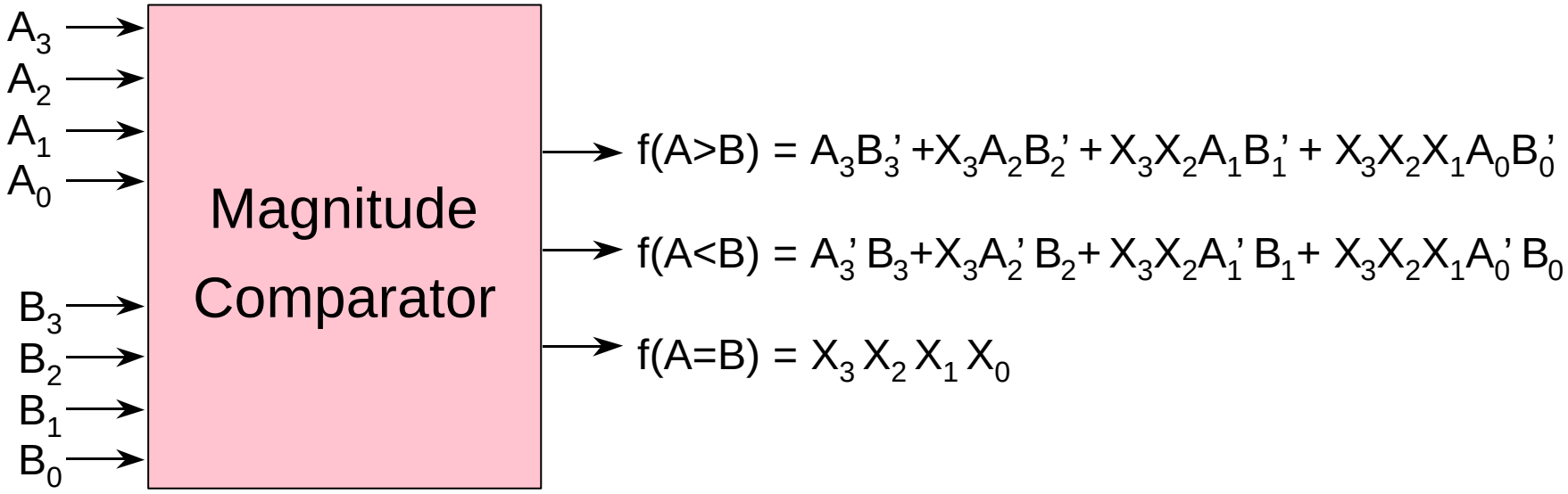
Magnitude Comparator

❑ 이진수 $A= A_3 A_2 A_1 A_0$ 와 $B= B_3 B_2 B_1 B_0$ 의 크기비교

$X_i = A_i \odot B_i$



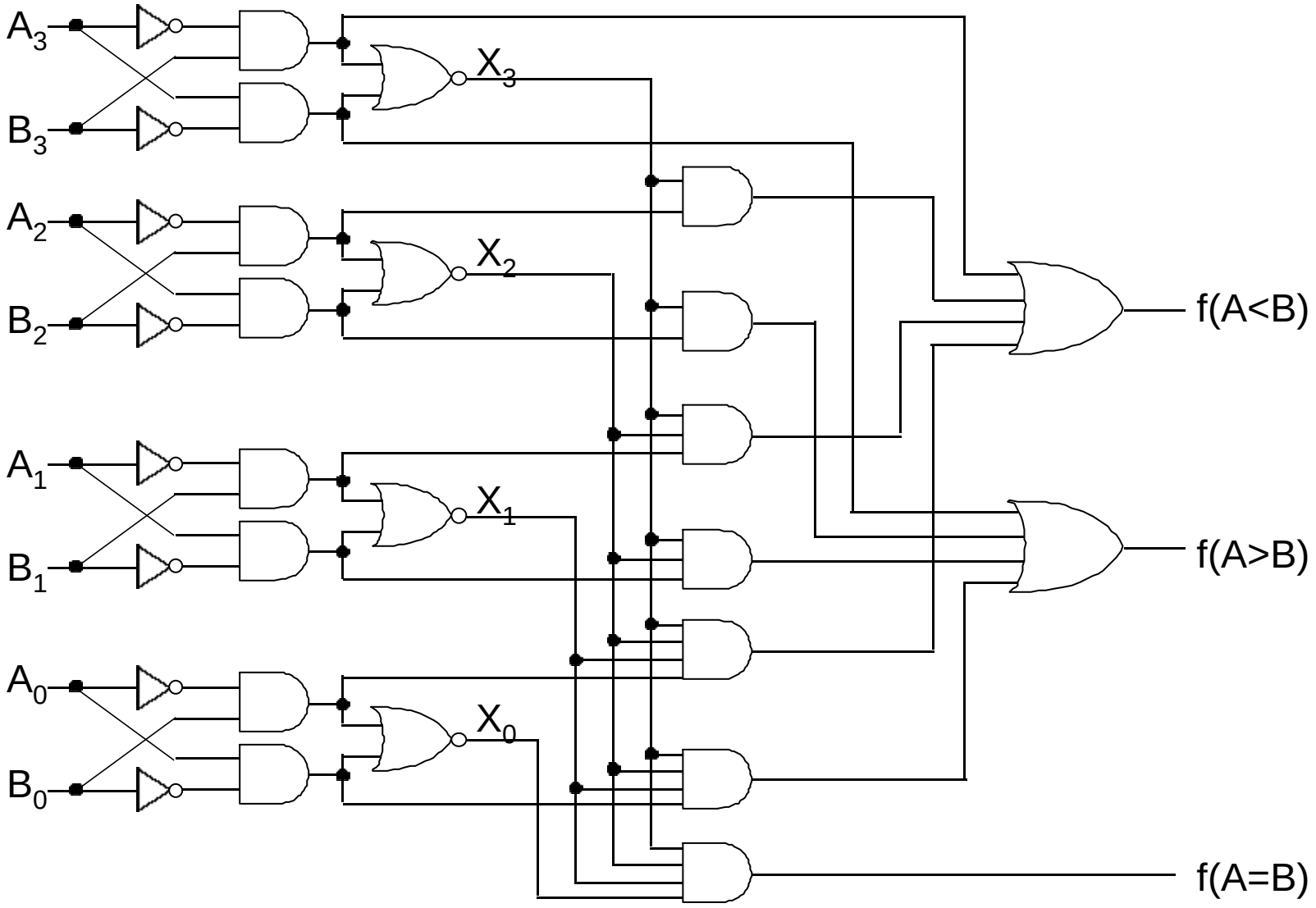
❑ A > B 인 경우

A : 1XXX △1XX △◇1X △◇☆1

B : 0XXX △0XX △◇0X △◇☆0

A_3B_3' $X_3A_2B_2'$ $X_3X_2A_1B_1'$ $X_3X_2X_1A_0B_0'$

Magnitude Comparator의 회로도



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