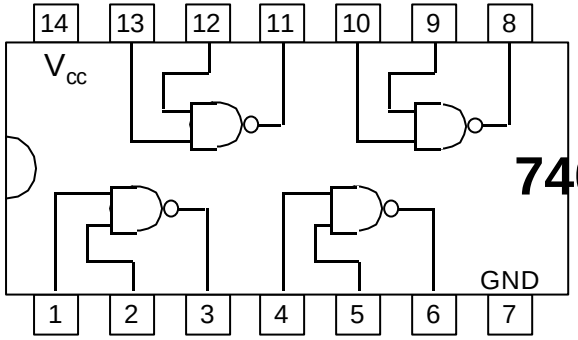
Integrated Circuits

- 논리게이트를 집적화하여 하나의 칩에 구현
  - SSI(Small Scale IC)
    10개 이내의 게이트 / 칩 (기본 게이트)
  - MSI(Medium Scale IC)
    수십개의 게이트 / 칩 (디코더, 카운터)
  - LSI(Large Scale IC)
    수백개의 게이트 / 칩 (ALU)
  - VLSI(Very Large Scale IC)
    수천-수만개의 게이트 / 칩 (CPU, Memory)
  - ULSI(Ultra Large Scale IC)
    수십-수백만개 이상의 게이트 / 칩(고성능프로세서)
  - GSI(Giant Large Scale IC)

Commonly used 7400-Series SSI ICs



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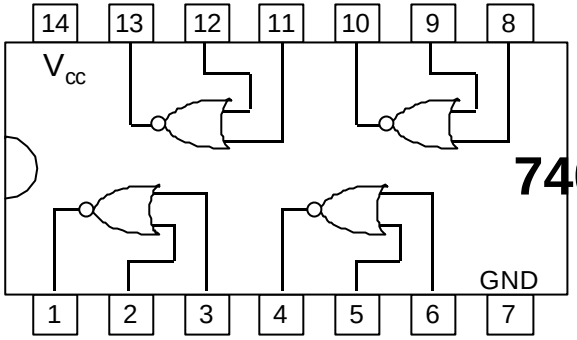

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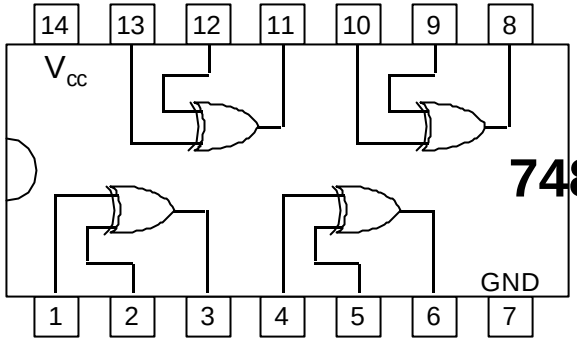

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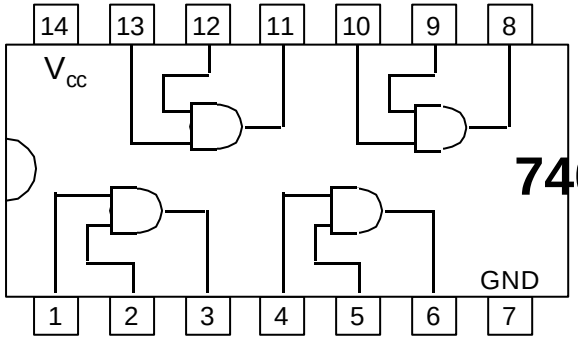

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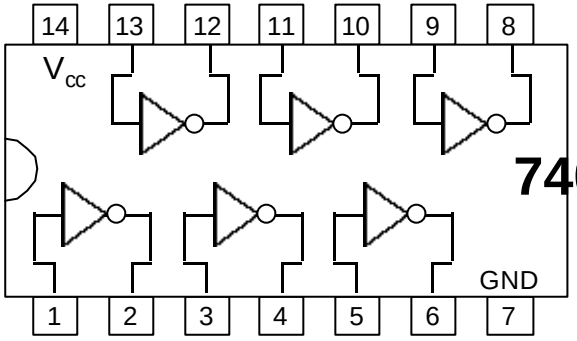

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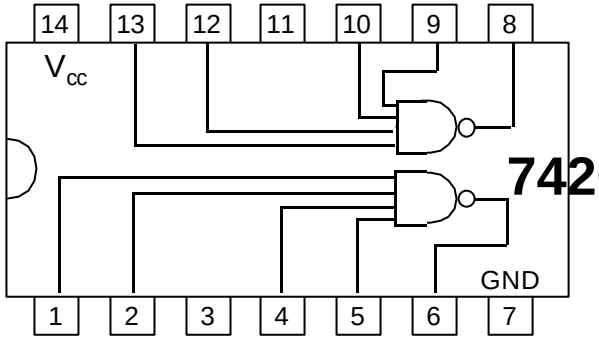

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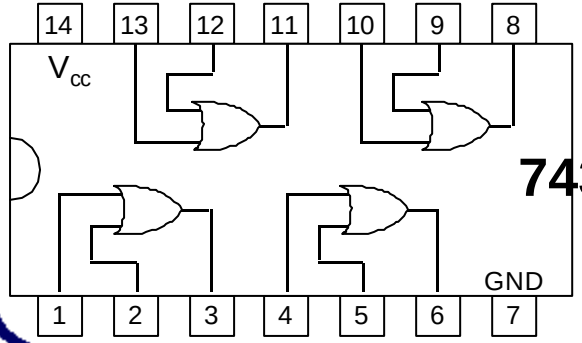

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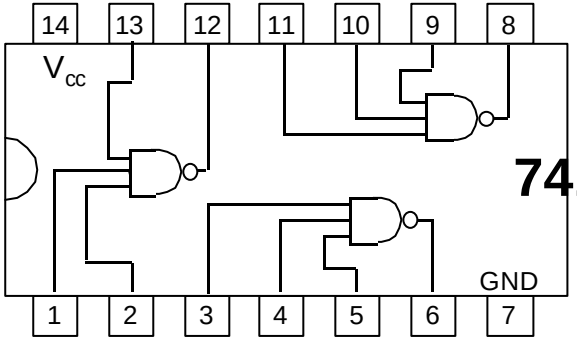

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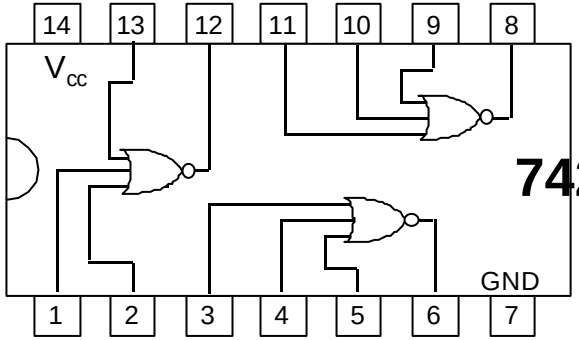

7427

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Positive Logic and Negative Logic

- Positive logic

- Negative logic

Positive logic AND

X Y	F
0 0	0
0 1	0
1 0	0
1 1	1

Positive logic OR

X Y	F
0 0	0
0 1	1
1 0	1
1 1	1

Negative logic AND

X Y	F
0 0	0
0 1	1
1 0	1
1 1	1

Negative logic OR

X Y	F
0 0	0
0 1	0
1 0	0
1 1	1

- Positive logic AND = Negative logic OR
- Positive logic OR = Negative logic AND

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Characteristics of IC Logic Family

- Fanout
  - 정상동작에 영향을 주지않고, 게이트의 출력에 걸어 줄 수 있는 부하의 갯수
- Power dissipation
  - 게이트를 동작시키기 위해 필요한 전력
- Propagation delay
  - 입력측의 신호가 출력측에 전달되기 까지 걸리는 시간
- Noise margin
  - 입력신호에 포함될 수 있는 잡음의 최대 허용치
- Degree of integration
- Component cost

IC Digital Logic Family

- RTL (Resistor Traansistor Logic)
- DTL (Diode Transistor Logic)
- TTL (Transistor Transistor Logic) : **보편적으로 널리 쓰임**
- ECL (Emitter Coupled Logic) :**고속 동작에 적합**
- MOS (Metal Oxide Semiconductor) : **고집적도**
- CMOS (Complementary Metal Oxide Semiconductor) : **고집적도, 저전력**
- I^2L (Integrated Injection Logic) : **고집적도**
- BiCMOS

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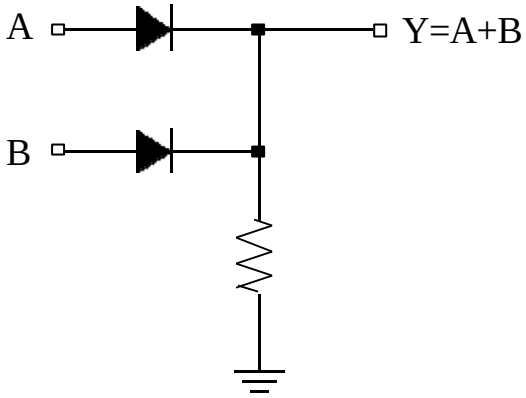
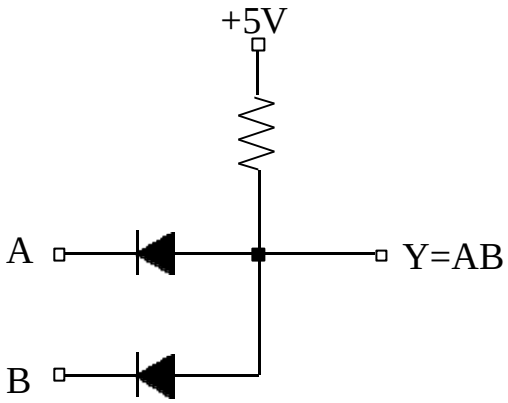
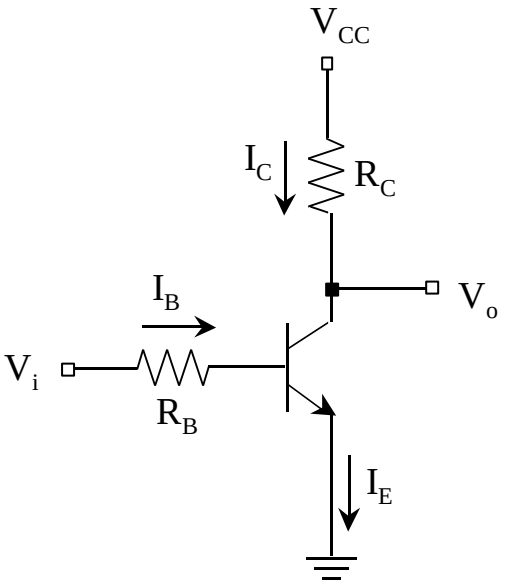
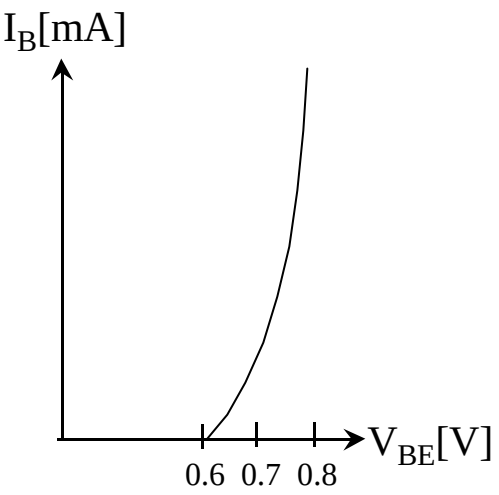
Diode Logic

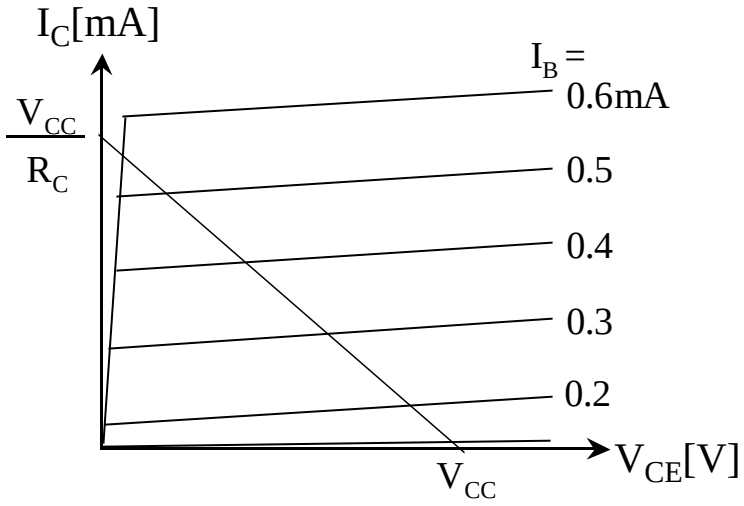




Bipolar Transistor







Region	V_{BE} [V]	V_{CE} [V]	Current Relationship
Cutoff	< 0.6	Open circuit	$I_B=I_C=0$
Active	0.6 - 0.7	> 0.8	$I_C=h_{FE}I_B$
Saturation	0.7 - 0.8	0.2	$I_B >> I_{CS}/h_{FE}$

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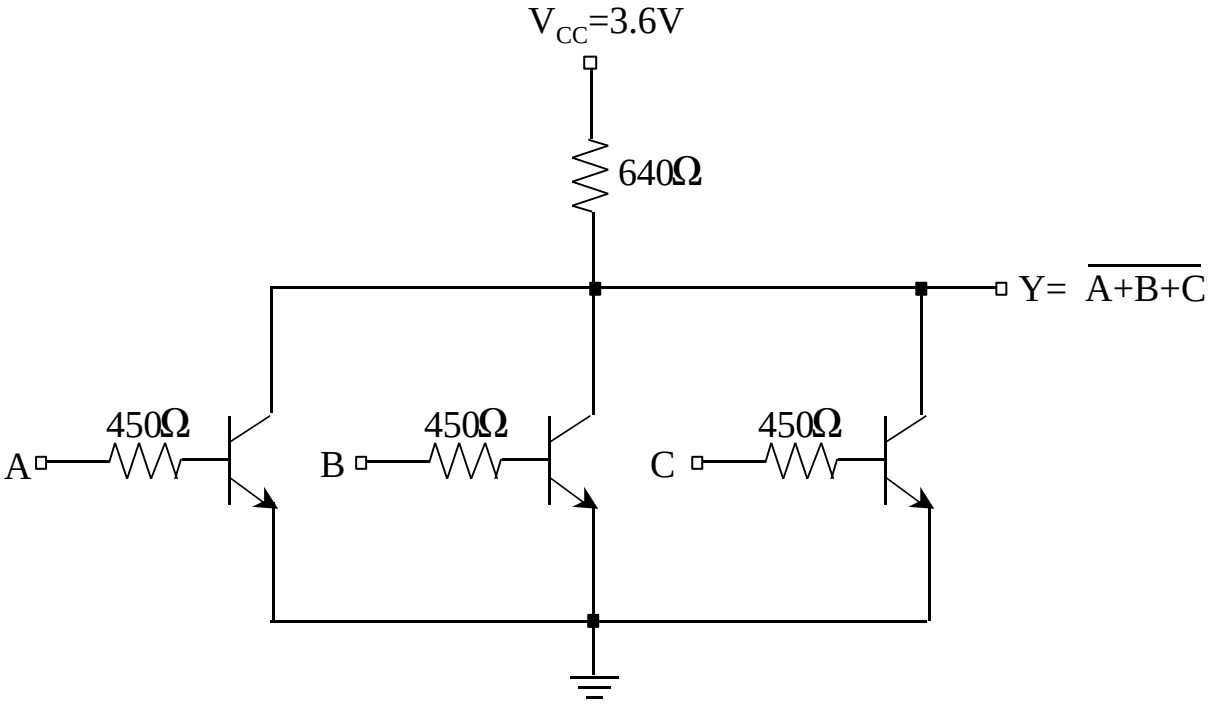
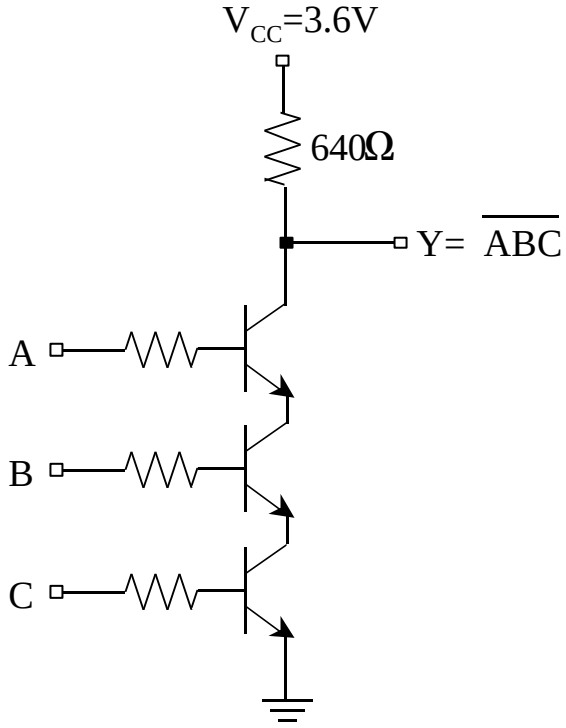
RTL(Resistor Transistor Logic)

- L:0.2V, H:1.0-3.6V
- Power dissipation:12mW
- Propagation delay: 25ns
- Noise Margin: 0.4V
- Fanout= 5





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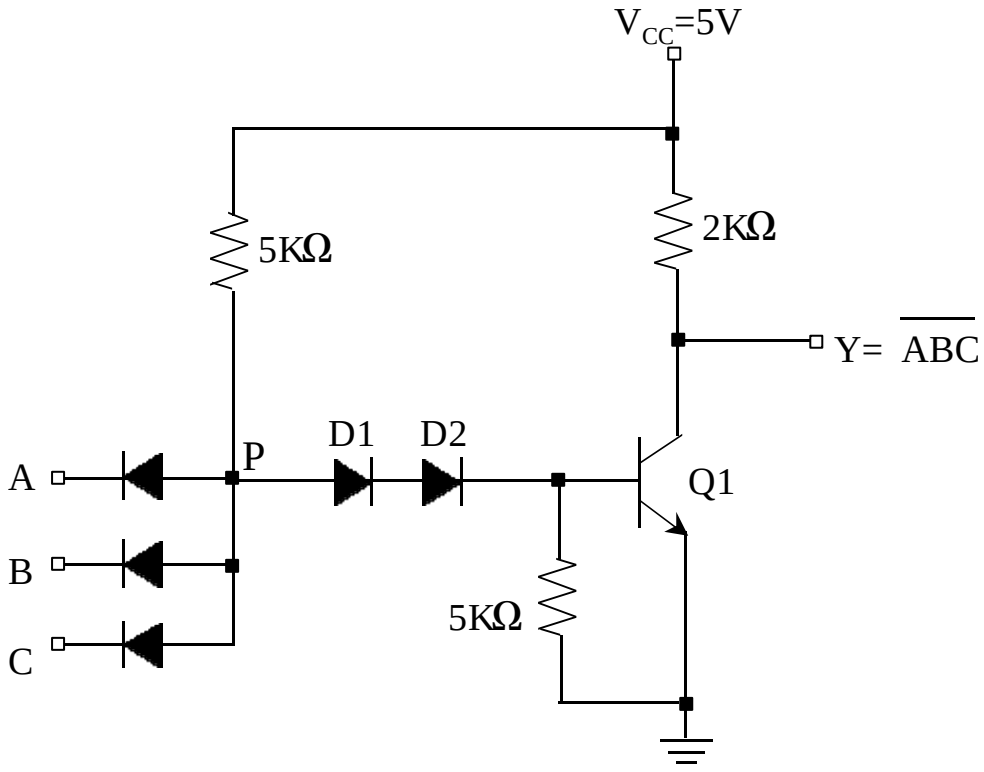
DTL(Diode Transistor Logic)

- L:0.2V, H:4-5V
- Power dissipation:12mW
- Propagation delay: 30ns
- Noise margin: 1V
- Fanout: 8



- A,B,C중 하나가 L 이면
  → P=0.2+0.7= 0.9V
  Q1이 ON되려면 P는 최소한
  P= 0.7+0.7+0.7= 2.1V
  ∴ Q1 is OFF → Y=5V
- A,B,C모두 H 이면
  Q1 is ON → Y= 0.2V

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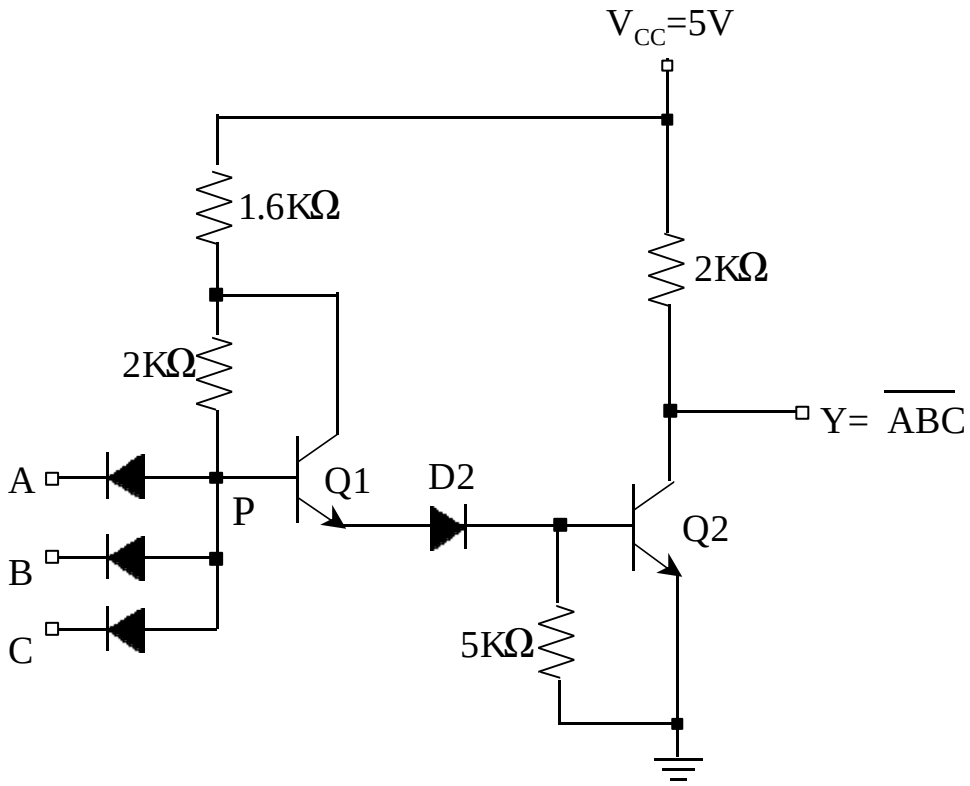
DTL의 변형



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TTL(Transistor Transistor Logic)

TTL series name	Prefix	Fanout	Power dissipation [mW]	Propagation delay [ns]	Speed-Power product [pJ]
Standard	74	10	10	9	90
Low-power	74L	20	1	33	33
High speed	74H	10	22	6	132
Schottky	74S	10	19	3	57
Low-power Schottky	74LS	20	2	9.5	19
Advanced Shottky	74AS	40	10	1.5	15
Advanced low-power Schottky	74ALS	20	1	4	4

- TTL output
  1) Open-collector output
  2) Totem-pole output
  3) Tristate output

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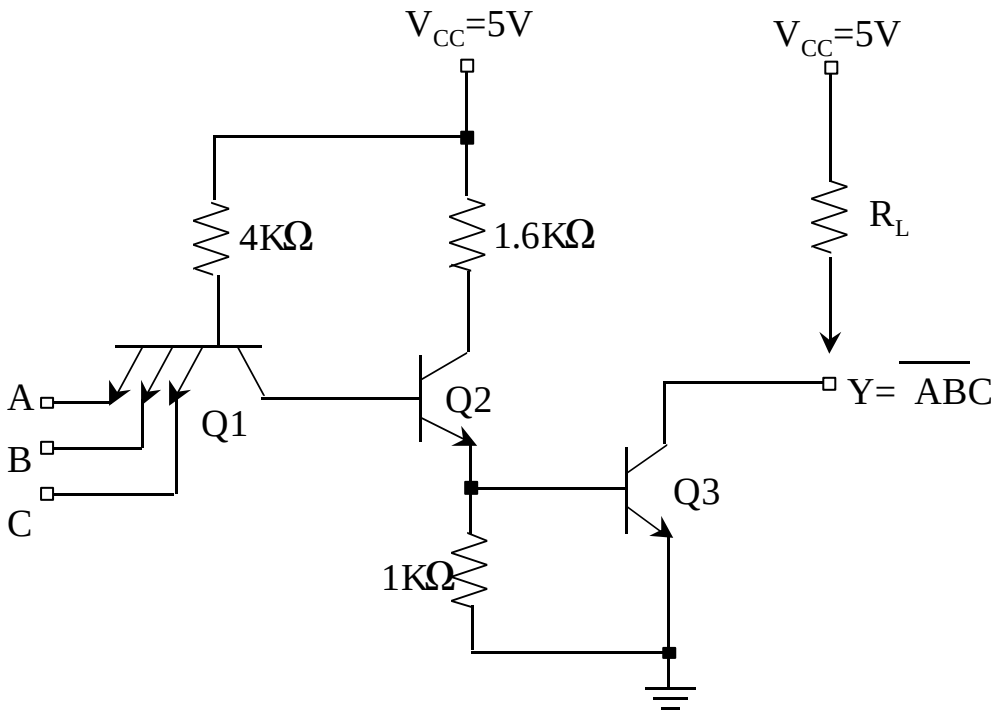

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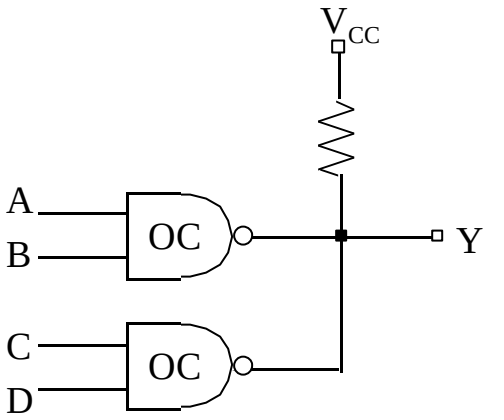
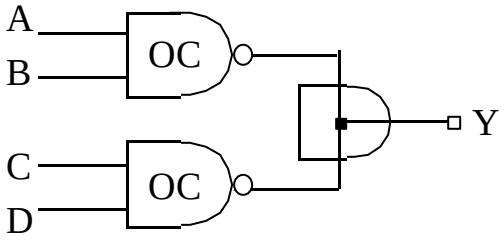
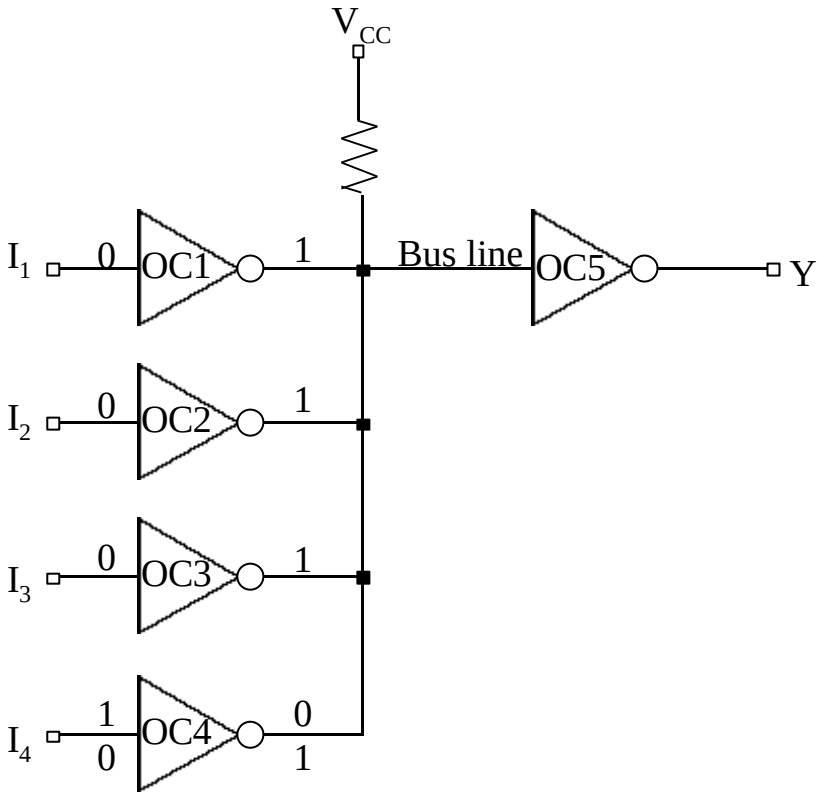
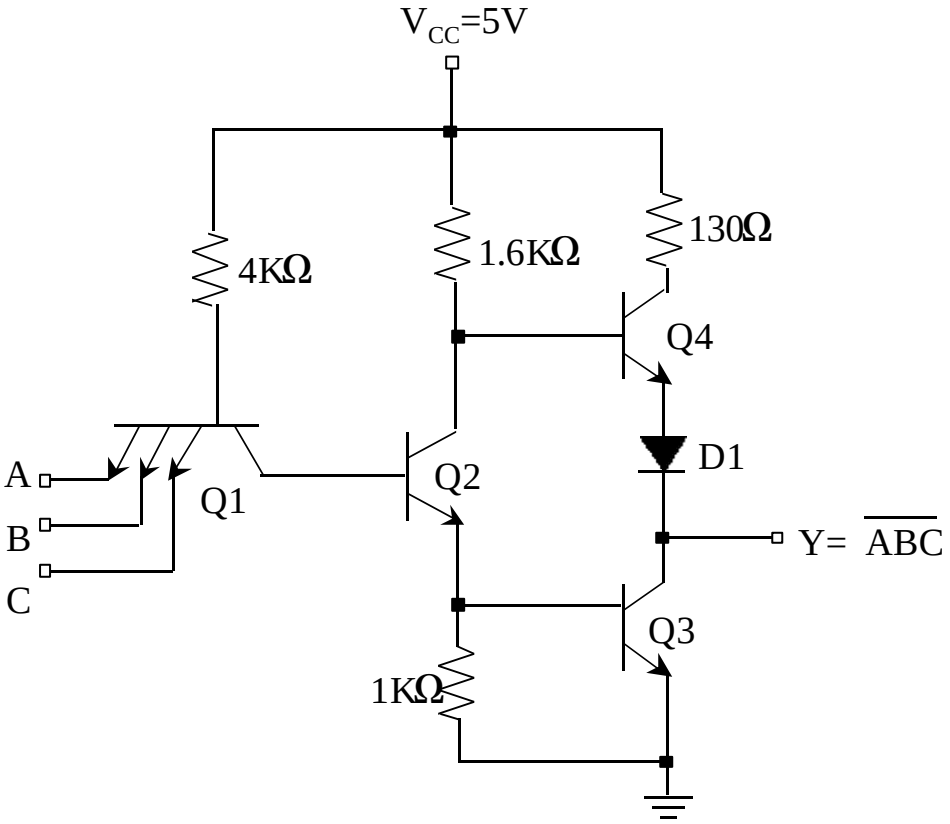
Open Collector TTL







Totem-Pole Output TTL



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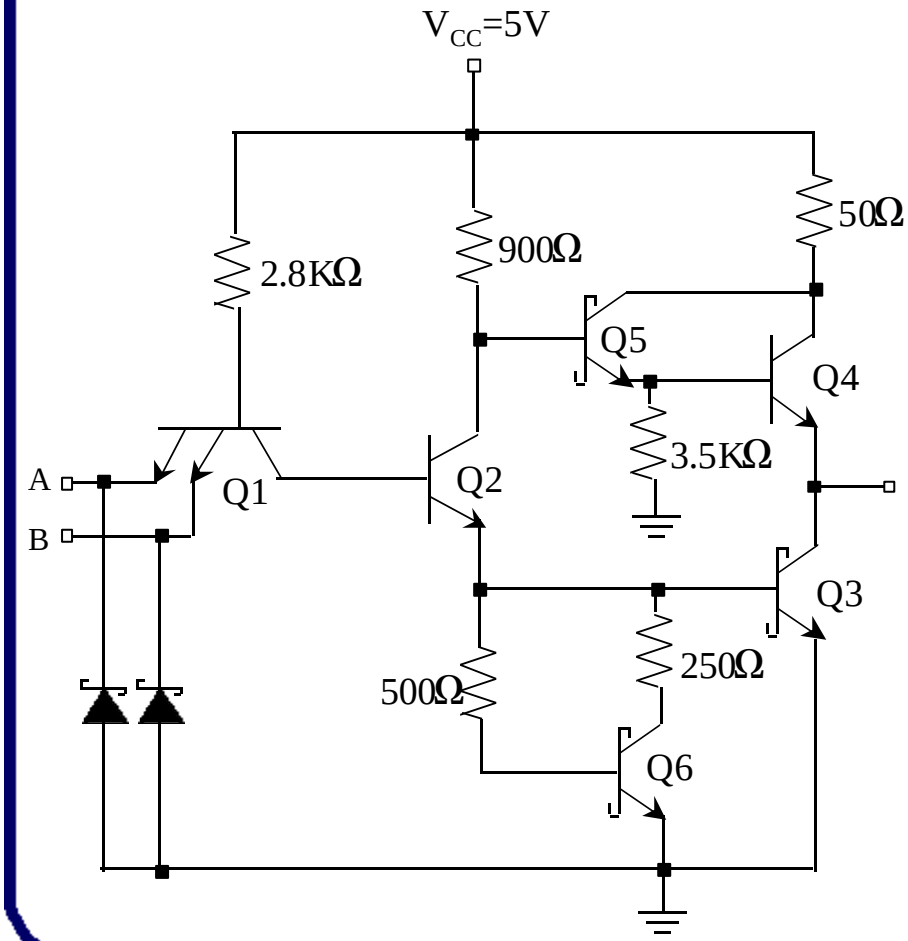
Schottky TTL



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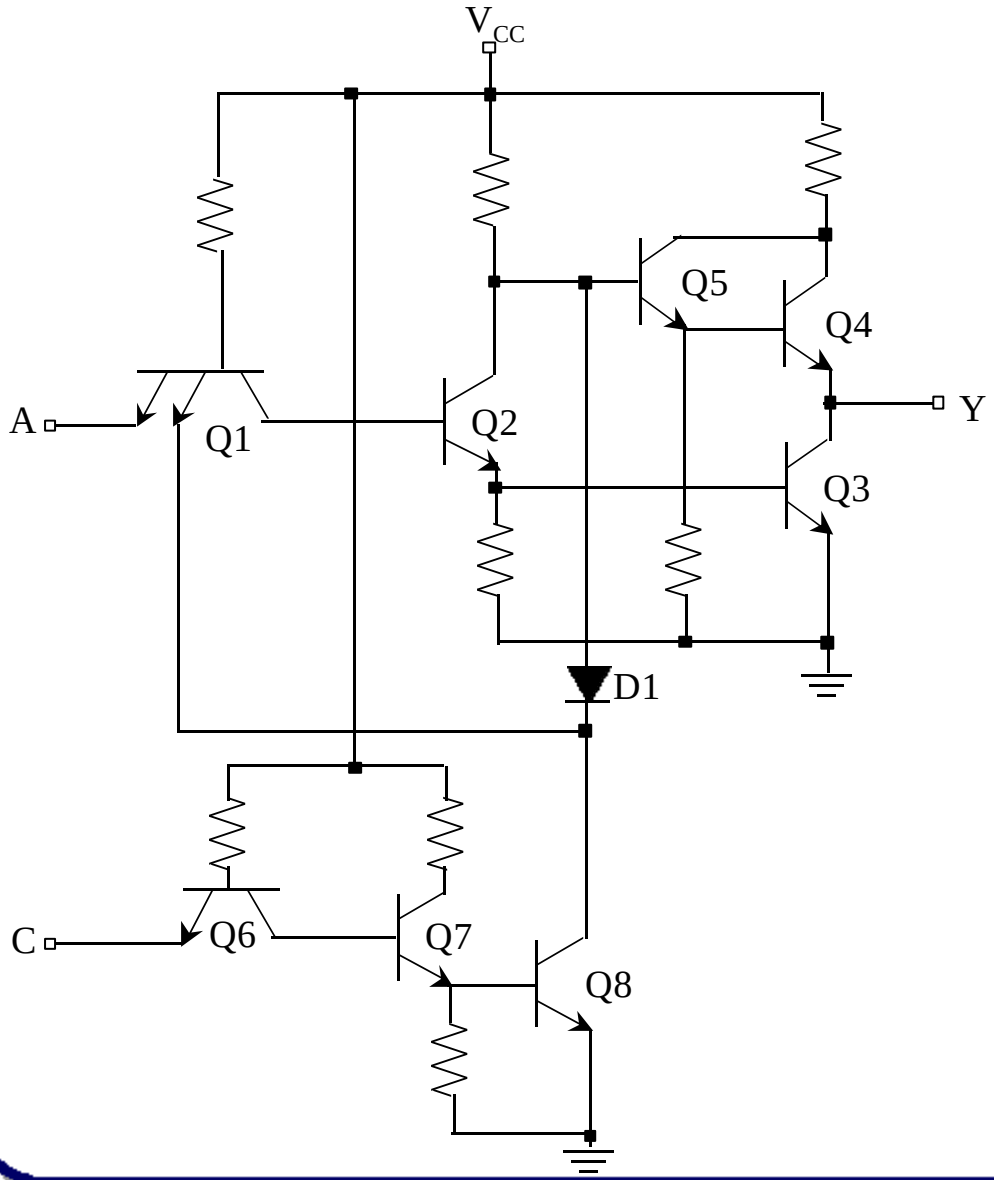
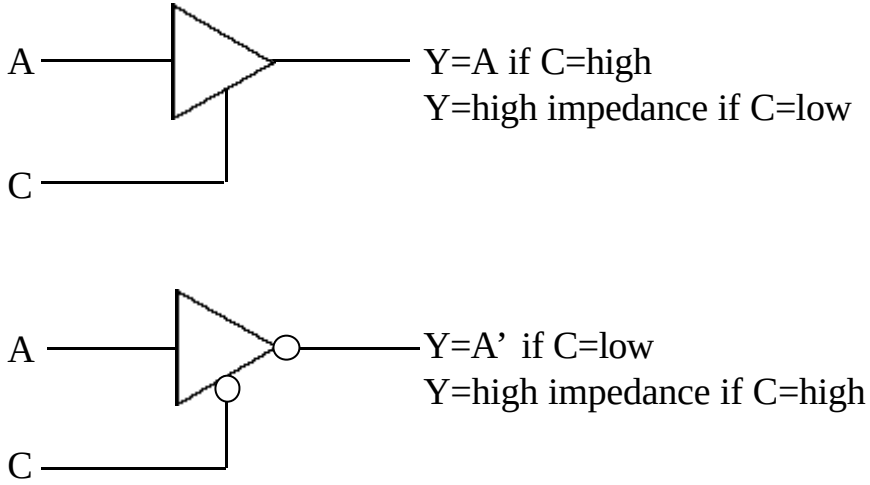
3-State TTL Gate





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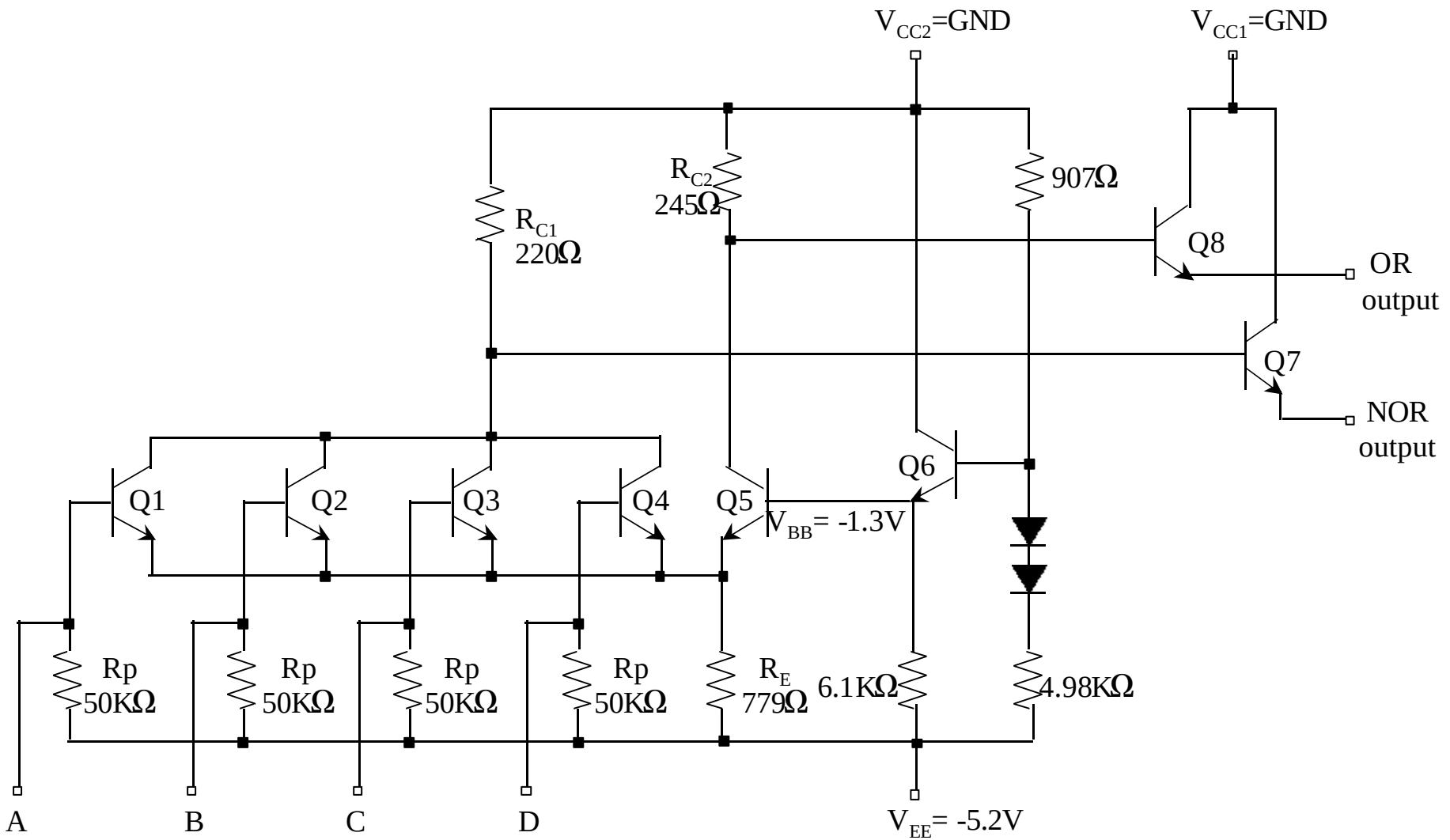
ECL(Emitter Coupled Logic)



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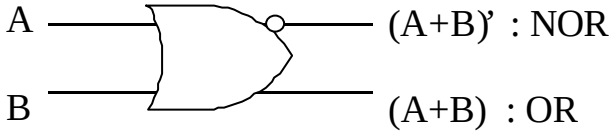
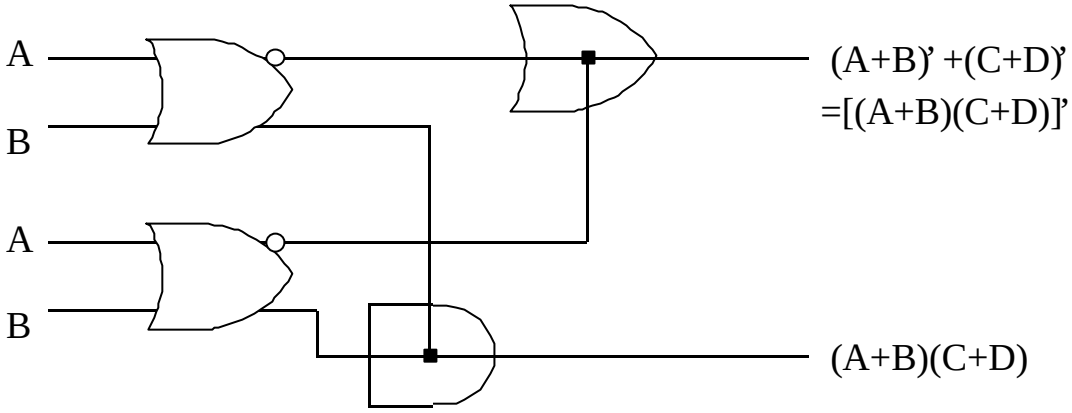
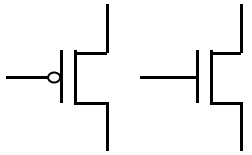
ECL gates





CMOS Logic Gates



CMOS

CMOS Logic Gate

Transmission Gates